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MANUFACTURER: NARCO

MODEL: DME 890 DISTANCE MEASURING EQUIPMENT

TYPE OF PUBLICATION: MAINTENANCE MANUAL

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NARCO AVIONICS DME 890 DISTANCE MEASURING EQUIPMENT



MAINTENANCE MANUAL

NARCO AVIONICS INC.

FORT WASHINGTON, PENNSYLVANIA, 19034 U.S.A.

ATP RECORD OF REVISIONS

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MOD. INSTR. #03225-0670		Nov./81	Dec. 30/81	ATP			
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RECORD OF TEMPORARY REVISIONS

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NARCO AVIONICS

DME 890

(MM - 03314-0600 dtd 12/80)

IS YOUR MANUAL COMPLETE?

This page is provided, and updated as necessary, with each printing and supplement issued. As all pages are dated, it is easy to verify if the manual on hand is complete and current. Page numbers prefixed by a "B" are pages that are intentionally blank.

A complete page by page check can be made by comparing the page number and date below to that of each page. A quick check can be made by "eyeing" the bar(s) at the base of this page against the

bottom edge of the whole manual. One bar on this page indicates one set of supplemental pages were issued, additional bars. . . additional supplements. Generally one will eye at least one bar per supplement.

It should be noted that the pages of Sections 1 and 2 may be dated prior to the cover date of the Maintenance Manual as those Sections are the Installation Manual which always preceeds the Maintenance Manual.

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NARCO AVIONICS DME 890

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1.1 INTRODUCTION

This manual is intended to provide accurate information pertaining to the installation and maintenance of Narco Avionic's solid state/digital readout DME 890.

1.2 MANUAL ORGANIZATION

Section 1, INTRODUCTION: defines the scope of the manual, its broad content, how to use, and a consolidated listing of the DME 890's features.

Section 2, INSTALLATION: provides specifications, wiring diagrams, and mechanical procedures to install the unit. Section 2 also includes both electrical and mechanical adjustments that may be necessary to complete the installation. Operation procedures provided are directed to the installer/flight test pilot to allow quick orientation to the DME's use and readouts.

Section 3, CIRCUIT DESCRIPTION: this Section commences with a broad discussion of DME's in general and an indepth discussion of the DME 890. This broad discussion is followed by an indepth description of all the circuits of the Unit.

Section 4, MAINTENANCE: test equipment required, mechanical procedures to get to, remove, and replace major subassemblies and some specific components, is followed by YES-NO troubleshooting flow diagrams. Alignment procedures are also provided with a listing of all adjustable components and the setting of them.

Section 5, REPLACEMENT PARTS LIST: this Section is dedicated to listing and showing all mechanical parts (where possible) that are considered replaceable. Electrical parts not identified on printed circuit boards as well as those mechanically attached are also listed.

All electrical parts are listed on the reverse side of their related schematic in Section 6.

Section 6, SCHEMATICS: provides an internal electrical wiring diagram of the Unit, separate but related subassembly (pc board) schematics, and test information.

To the left of each subassembly schematic is its pc board identifying each component in position by its symbol number.

Note that both the printed circuit board and schematic are provided with grid coordinates. Refer to the Electrical Parts List on the reverse of the schematic, and in line with each electrical component, will be its pc board and schematic grid coordinates. The component's location is considered in that grid box wherein the symbol letter (i.e. CR101, U101) is located even though the graphic electrical symbol may be in a adjacent grid box.

1.2 Continued

Update schematics will also contain equivalent lists, however these will identify: added, changed, and deleted parts along with the Chassis Level Code identifying when that particular action was effected on the assembly.

1.3 INSTALLATION MANUALS

Installation Manuals are advance copies or, in effect, reprints of Section 1 and 2 of the Maintenance Manual. Should the user have an IM and MM of different dates (see cover), use the most current manual.

1.4 FEATURES:

- 100% modular solid state design...microprocessor controlled.
- Professional-style, gas discharge digital readouts.
- Instant station lock-on, typically less than 1 second.
- Distance accuracy -0.1 nautical mile (nominal) up to full range.
- Panel tuning controls----or optional automatic remote channeling
- Compact low profile, lightweight, self-contained
- 200 channels, 25 watts nominal
- Ident level control
- Fast servicing-easy to get to test points
- Automatic readout intensity control
- Track type mounting tray

2.1 GENERAL

The Narco Avionics DME 890 is self-contained, operates from either 14 or 28 Vdc, and is designed to be mounted in a standard aircraft instrument panel radio rack.

The DME's tray is of rail design which provides full length support to the DME. The tray contains a new type of locking device actuated by a pin type key.

The antenna, Narco's standard UDA-3 is provided in the overall DME 890 package.

2.2 UNITS AND ACCESSORIES SUPPLIED

The following list identifies the DME 890 system and the order number to use to obtain the complete system. Individual items of the system may be ordered using the part numbers listed opposite the individual item.

ITEM	ORDER NUMBER	DESCRIPTION	PART NUMBER
1	03314-0300	DME 890 System (Unit, Tray, Antenna, Inst. Kit)	
		Individual Items: DME 890 Tray Assy Installation Kit Antenna UDA-3	01380-0101 01372-0103 03314-0500 01063-0102

INSTALLATION KIT

Item	Part Number	Description	03314- 0500	See Figure
1	56912-0001	Key, Spring Release	1	2-4
2	50042-0001	Tool, Tray Side Rail Spacer	1	2-5
3	50043-0001	Shim, Side Rail	2	2-5
4	41407-0002	Pin, Connector - Strip	24	2-6/2-10
5	41273-0002	Connector, BNC (Plug)	2	= =
6	90072-0002	Cable, Coax, Low Loss, 10 FT.	1.	4.
7	99453-0001	Tie, Wire, 6 inch	1	= =

2.3 SPECIFICATIONS

2.3.1 Mechanical

Size:	DME 890 with mo										See Figure 2-3.
	UDA-3 Antenna		•.	٠	•	•	٠	٠	ě	•	See Figure 2-11.
Weight:	DME 890	•	•								3.30 lb 1.375 kg
11	Mounting Tray						1100				.63 lb .288 kg
	Antenna/cable										.5 lb .21 kg

2.3.2 Electrical

Power requirements
Transmitter frequency band 108.00 thru 117.95
paired with 1041 thru 1150 MHz
Transmitter power
Transmitter frequency stability less than .01%
Number of channels
Receiver frequency 108.00 thru 117.95
paired with 978 MHz thru 1213 MHz
Receiver sensitivity82 dBm min
Acquisition time, including channeling 1 second
Range
Memory
Ident audio output 10 mW, typical
Digital outputs 160.0 nm in 0.1 nm steps
Digital outputs
Ground speed accuracy5 knots or -5% (std signal
conditions)

2.3.3 Environment

Temperature I	Range									
Non operati	ing -Low	٠							-40°C	$(-40^{\circ} F)$
	-High	•		٠				·	+70°C	$(158^{\circ}F)$
Continuous	Operation	1								
	-High				٠	٠		•	+55 C	(131°F) (+5°F)
	-Low		100	٠					-15°C	(+5°F)

Below 0°C some degradation in output power may occur, primarily at the band edges. In a cabin environment, Unit internal temperature will rise to 0°C in approximately 15 minutes.

Altitude:

Non-pressurized	•	•			•	•				•	٠			50,000	FT.
Pressurized			•								•	K I		50,000	FT.
Not affected by	de	eco	omj	pr	es	sic	on	to)		•			50,000	FT.

11 32 Vda 15W

2.4 PREINSTALLATION BENCH TEST

2.4.1 Test Equipment Required

As numerous test equipments are being introduced yearly and many exceed our requirements, the unit(s) referred to are typical and/or minimal in vintage and scope. Refer to Narco's Service Center Handbook for "required equipment" detail listings.

Therefore this list identifies test equipment by functional name and the predominant function required of the unit to be used in making the test. Where names and model of units are expressed, that unit, or one that is at least as equivalent must be used.

- a) Power Supply, 5 amp 0/28 Vdc
- b) Test Generator, IFR 1200Y3
- c) Oscilloscope
- d) Headphones or Speaker

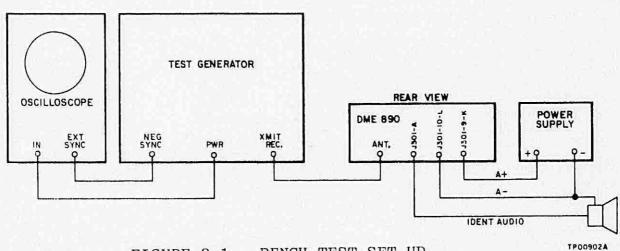


FIGURE 2-1. BENCH TEST SET-UP

2.3.2 Procedure

Refer to Figure 2-1 and 2-2.

Should the Unit fail to meet the following tests, refer to Section 4 for troubleshooting and repair procedures.

- a) Turn the DME's switch to OFF
- b) Connect test equipment and DME.
- c) Set test generator to 100 nm range, attenuator to -73 dBm, reply efficiency to 70%, and squitter to 2700. Set power supply to aircraft's A+ voltage (14 or 28 Vdc). Set DME's mode switch to FREQ.
- d) Then energize the DME by turning the knob into the IDENT (volume) area.

2.4.2 Continued

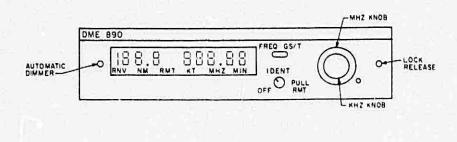


FIGURE 2-2. DME 890 PANEL

e) Verify that the MHz lamp readout segments illuminate in a sequential manner through its 108 to 117 range by rotating the MHz frequency Knob.

TP00903

- f) Verify that the KHz lamp readout segments illuminate in a sequential manner through its .00 to .95 range by rotating the KHz frequency Knob.
- g) Verify that the letters MHZ are illuminated during steps e and f.
- h) Set DME 890 and test generator to the same channel (i.e. 112.50 MHz)
- i) Verify that the DME's distance readout reads 100 (-.2 nm) and that the letters NM are illuminated.
- j) Set test generator speed to 240 knots, direction inbound.
- k) Set DME 890 mode switch to GS/T.
- 1) Start test generator tracking.
- m) Transmit power should read 30 watts, nominal.
- n) Allow ground speed to stabilize (about five minutes), then read the knots. This readout should be within -5% of that indicated on the test generator and that the letters KT are illuminated.
- o) Check Time-To-Station accuracy. TTS should be within -1 digit of the following formulas answer:

 Distance (DME 890) ÷ 4 = TTS

- p) Change the DME 890's frequency off of 112.50 and verify that the KT and MIM displays will switch over and read the new frequency. The distance readout should BAR. Return DME to 112.50.
- q) Remove the RF signal from the DME. Verify that, in approximately 10 seconds, the distance readout will BAR and then the KT and MIN displays will drop out (change) and be replaced by the set frequency, 112.50.

2.4.2 Continued

r) Activate the remote channeling switch (pull out) and verify that the display flashes the word Error (Error). This appears in the readout in place of the frequency. The RMT letters should be illuminated.

NOTE: this test assumes no remote channeling connections.

s) De-activate the remote channeling switch (push in).

t) Check IDENT operation on ALL KHz channels. (The volume level is controlled by the potentiometer section of the ON/OFF switch).

u) Check IDENT operation on ALL MHz channels for power and

lock-on.

v) Check sensitivity during tracking. DME should track at -82 dBm.

w) Check the automatic dimmer's operation by covering light cell opening - displays intensity should go low. Shine a light into the cell, displays should appear brilliant.

x) RNAV illumination can be achieved by grounding pin J of

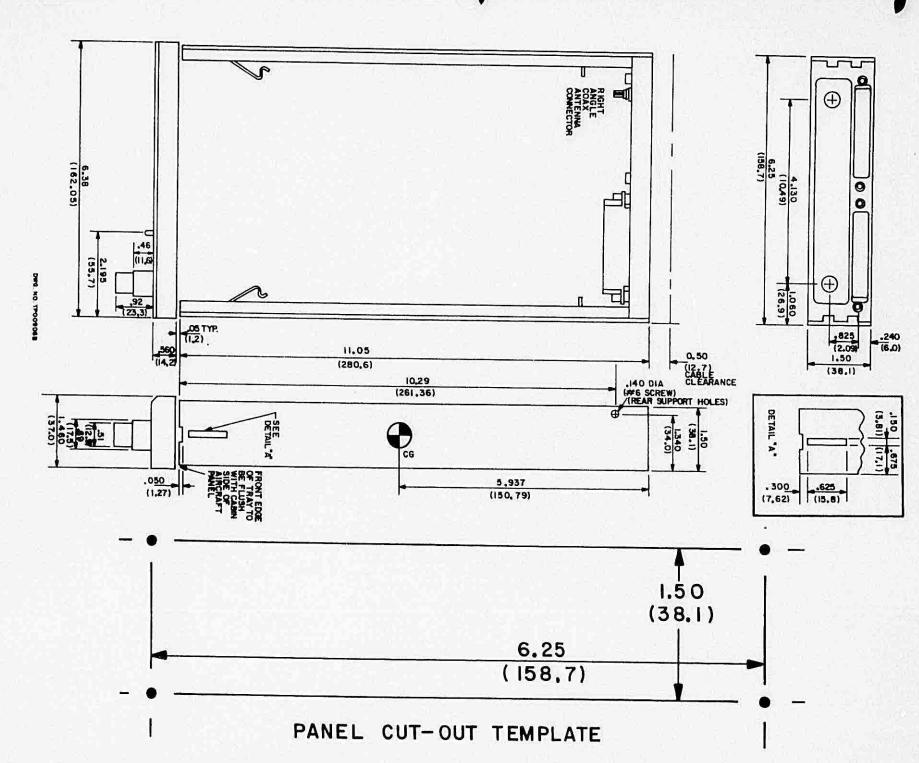
P301 (rear connector).

Test complete, turn DME OFF, disconnect set-up.

NOTE: The digital system of the DME 890 operates statistically on a TACAN or DME signal. Some test generators do not accurately simulate the ground DME or TACAN signal and may not operate the DME 890 correctly. The result is improper distance or ground speed computation. This is usually caused when squitter or countdown is not produced in a random manner.

(2-8)

2-7 Blank)



2.5 INSTALLATION

This Section provides the mechanical installation steps for mounting the tray and the wiring at the rear connector. Also provided are the instructions to install the UDA-3 Antenna.

2.5.1 Tray Lock

The tray has a built-in spring locking device. When the Unit is positioned into the tray's track and slid into the tray a tension, locking, spring contacts the Unit. When the Unit's connector(s) touch the tray connectors an additional set of tension springs can be felt holding back the inward direction of the Unit. At this point using firm pressure the Unit will continue inward approximately a half-inch stopping as the forward tension/locking spring "clicks" into position. The Unit is now locked in place.

Removal of the Unit requires an extraction tool. Place the tool into the small hole provided in the right corner and push into the hole. This action clears the forward tension spring from the locking detent, and due to the rear springs, the Unit will "pop" outward an inch or two. The Unit is now disconnected from the rear connector(s) and the tray lock, and is ready to be slid out of the tray.

2.5.2 Mechanical - Tray

Upon removing the DME 890 from its shipping container, the Unit must be removed from its mounting tray.

Position the assemblies on a flat surface, place a block behind it as shown in Figure 2-4. Insert the key straight into the key hole in the trim panel, exert sufficient pressure to release the spring lock. Upon release the tension (eject) springs will "pop" the Unit outward, freeing it. Save the key.

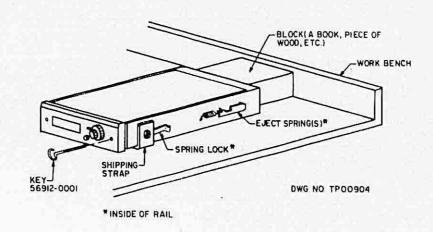


FIGURE 2-4. TRAY LOCK

2.5.2 Continued

Prepare the panel cutout for the tray. Refer to Figure 2-3 that provides dimensions and a 1:1 template.

The proper position of the tray, when installed, is that where the edges of the side rails on the open end of the tray will be flush with the cabin side of the instrument panel.

For convenience, if you are going to remove the connector, mark a piece of tape "TOP" and apply it to the top of the mounted connector (P301) before removing it.

Remove the "U" shipping strap (see Figure 2-4) from the tray. SAVE THE SCREWS, discard the strap and nuts. Handle the tray with care to avoid deforming the rails.

The installation kit contains a Rail Width Tool. It was designed to provide a exact width for optiumum unit/tray fit. This tool is to be positioned during tray installation touching the back of the nylon blocks on the rails (2-9/16 inches) in. The "U" shims in the kit are used to fill voids between the forward mounting supports and the Rails (if required). Due to their simplicity, if additional shims are required, they can be quickly fabricated by the installer.

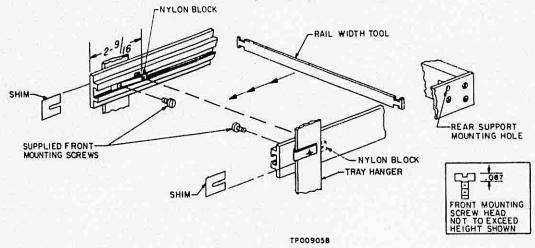


FIGURE 2-5. TRAY FRONT WIDTH

Attach these ends using the screws that attached the shipping strap. Should any other screws be used its head <u>cannot</u> be more than .087 high as should it be higher it may be nearly impossible to remove the unit as the KEY must be able to pass between the screw head and the Unit to disengage the spring lock! NOTE: DO NOT USE LOCKWASHERS. Locking "J" nuts or equivalent should be used. Rear support should be provided using the .140 inch diameter holes shown on the side rails (see Figure 2-3).

Note that the screw head height is very critical a larger head screw will allow the Unit to slide in, but the key will not pass.

2.5.3 Electrical Installation

Refer to Figure 2-6 thru 2-9 for appropriate connector wiring.

Use the Molex Crimp type contacts supplied. Refer to crimping method detailed in Section 2.5.3.1.

Before reinstalling connector previously removed, check that the cable leads were properly installed and that the key is in the correct position. Slide the connector through the opening. check that the marked side is on top, then secure.

ELECTRICAL INSTALLATION

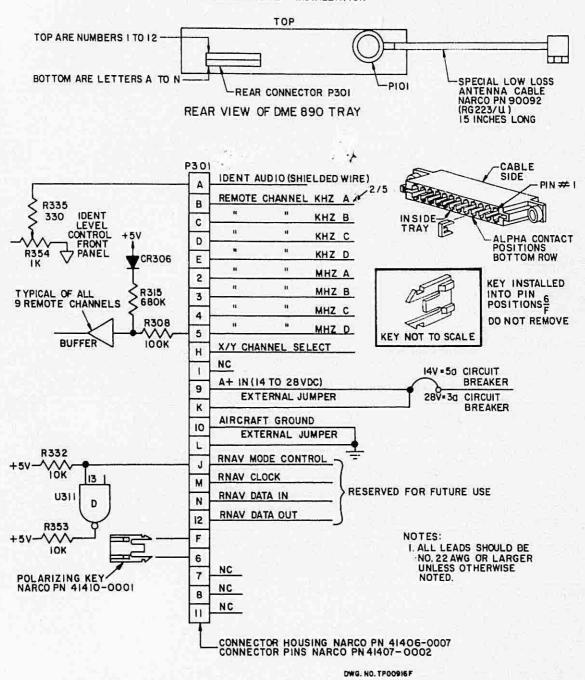


FIGURE 2-6. DME 890 REAR CONNECTOR WIRING

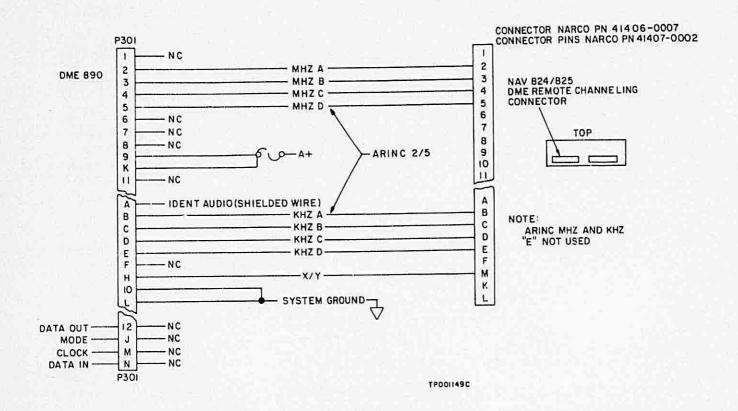


FIGURE 2-7. DME 890 WITH NAV 824/NAV 825

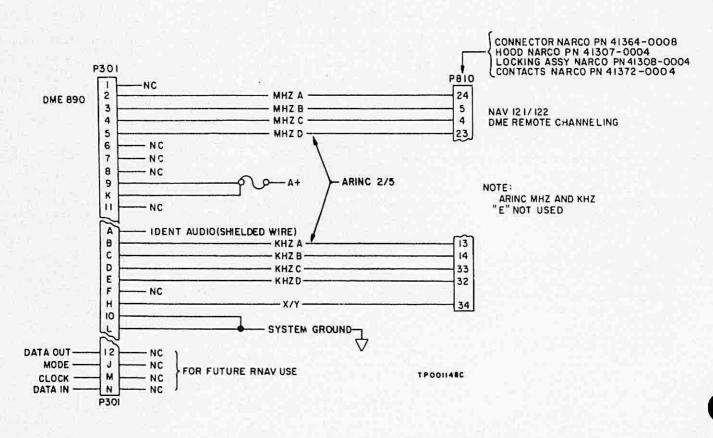


FIGURE 2-8. DME 890 WITH NAV 121/NAV 122

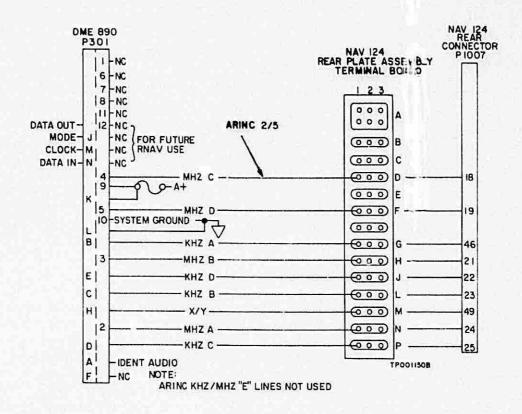


FIGURE 2-9. DME 890 NAV 124

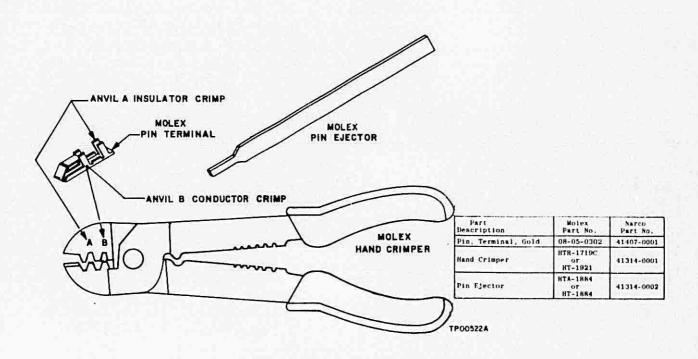


FIGURE 2-10. CRIMPING TOOL

2.5.3.1 Cable Fabrication

1. Strip wire 5/32" for each PIN connection.

2. Open tool (engraved side toward you), from the opposite side, place the conductor tab section of the pin on Anvil B. Close tool slightly (until tabs touch the female jaw).

3. Insert stripped conductor until insulation is flush with outside of jaw. Crimp by squeezing handles together until jaws are fully closed or sufficient crimp is made.

4. Move leads and pin to Anvil A. Crimp again until jaws are closed or sufficient crimp is made, so that insulation on

wire is crimped.

5. If necessary, straighten pin while still being held in the jaw.

Insertion

1. The PIN terminal may now be inserted into the desired pin location in the connector housing. The pin cannot be inserted upside down. Right-side-up it slides in effort-lessly. Be sure to push it all the way in, until a "click" can be felt, or heard.

2. There is no necessity to pull back on the lead itself except to test for the "locking feature", and then only

with a moderate pull.

Extraction

1. If a pin is erroneously inserted into the wrong housing position, or if at some later time a circuit change is desired, the pin can be removed easily. Slip the flat narrow blade portion of the ejection tool into the mating side of the housing, under the pin. This action picks up the locking key and allows the lead and pin to slip out of its position using a light pulling action in the lead. Neither pin nor position has been damaged allowing reinsertion in the same or another position.

2.5.4 Antenna

The Blade antenna, type UDA-3, is used for both receiving and transmitting by the DME. This antenna should be mounted on the bottom surface of the aircraft and located so that it is in the vertical position when the aircraft is in a level flight attitude. The mounting surface should be metal, electrically grounded, and extend at least 6" in all directions from the antenna connector. (See Figure 2-11). A three (3) foot minimum separation from other antennas, particularly transponders should be maintained.

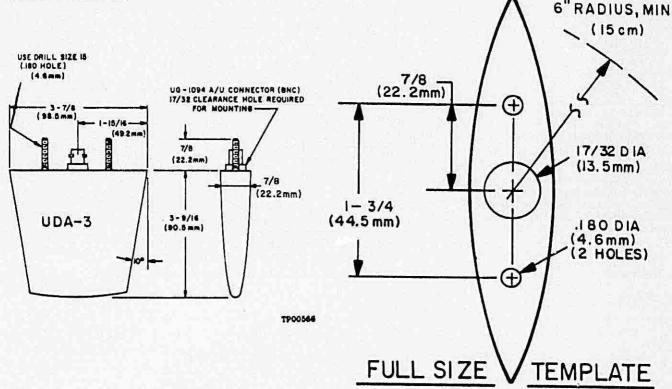
Avoid mounting the antenna in the vicinity of aircraft protrusions as this is likely to create some radiation "shadowing" with a resultant loss in signal strength from both transmitted and reply signals.

If this antenna is to be used on non-metallic aircraft skin, a ground plane at least 6" in diameter must be provided. This could be as simple as aluminum foil cemented inside a wood or fiberglass skin, or a doubler plate on a fabric-covered aircraft. Such a ground plane should be either well bonded to the airframe, or well insulated from it, to prevent erratic operation.

A doubler plate will be needed for an airworthy installation on most aircraft. Check the airworthiness regulations of the country of aircraft registry for acceptable mounting methods. Figure 2-11 is removable for a drilling template.

DO NOT PAINT. This antenna may not be coated with any paint or other finish.

6"RADIU



2.5.4.1 Antenna Cable

A thirty (30) inch antenna cable comes assembled to the rear of the case. This cable may be extended by use of the low loss ninety-six (96) inch cable and the connectors supplied in the Installation Kit.

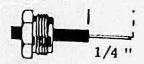
The cable run should be as direct as possible, having bend radiuses of 6 inches, minimum. In close areas a BNC 90 Adapter may be utilized to clear control cables in the vicinity of the antenna.

ANTENNA CABLE LOSS SHOULD BE KEPT AS LOW AS POSSIBLE. The length and type of cable is critical as the MAXIMUM cable loss should not exceed $1-1/2\ dB$.

KEEP THE CABLE AS SHORT AS POSSIBLE AND CUT OFF EXCESS LENGTHS! If it is necessary to run the antenna cable some distance or should the cable be changed, refer to the following examples and take note of their limitations.

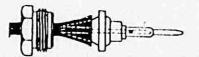
Cable Type	dB loss per 100 ft. @ 1000 MHz	Preferred length 1 dB or less	Maximum length 1-1/2 dB loss
RG 58 A/U	22. (.22 dB per ft)	4-1/2 ft	6 ft
RG 29 /U , RG 223 /U	17. (.17 dB per ft)	6 ft	8 ft
(90092) NARCO	16.4 (.164 dB per ft)	6 ft	9 ft 🔻
RG 54 A/U	11.5 (.115 dB per ft)	8-3/4 ft	11 ft
NARCO (90072)	10. MAX. (.10 dB per	ft) 10 ft	15 ft
RG 8 /U	8.5 (.085 dB per ft)	11-3/4 ft	17 ft

Figure 2-12 shows the proper method of connecting the BNC connectors to the antenna cable.

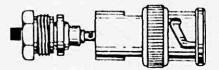


 Take one clean square cut through cable insulation, braid and dielectric, exposing ¼" of conductor Slip nut onto cable.

Coursesy of Bendix Corp.



 Insert conductor into tapered, selfclamping sleeve and contact subassembly, force edge of sleeve between dielectric and braid until insulation rides well onto taper. Solder conductor to contact at solder hole. Dwg No. TP00908



 Fit contact sub-assembly into connector body, screw nut into body, binding insulation and braid tightly against tapered sleeve. Thus forming a strong, weatherproof connection.

All illustrations enlarged for clarity

FIGURE 2-12. BNC CABLE CONNECTOR

2.6 OPERATION

This discussion is directed to the installer, and to the pilot who is to perform the flight test of the Unit.

Unless connected to a Remote NAV Receiver or an RNAV, the displays are controlled directly from the:

KHz/MHz continuous rotation knobs (CW/CCW)

OFF (ON/OFF) switch portion of the IDENT's potentiometer and its auxiliary RMT switch

FREQ GS/T (toggle) mode switch

When a Remote NAV Receiver or a RNAV have control, the RMT or RNAV display will light, as applicable.

TYPICAL DISPLAYS:

ERROR

This display is the result of the PULL RMT switch being in the OUT position and there is no Remote NAV Receiver connected to the DME.

OR

The Remote NAV Receiver is connected, however, the NAV is not providing a valid code to the DME's microprocessor.

Toggle Switch Set To FREQ

As either frequency knob is rotated the NM portion of the display bars and the MHz portion identifies the frequency set at that time.

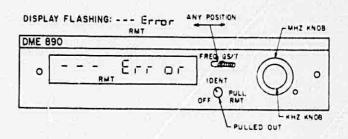
Once rotation ceases, and after lock-on (1 second or less), the NM portion displays the distance to the station.

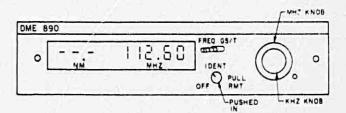
Toggle Switch Set To GS/T

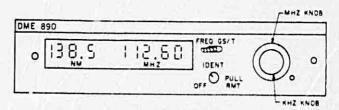
In the GS/T mode and locked-on to a station NMs, KTs, and MINs will be displayed.

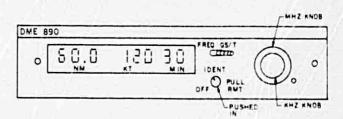
Frequency may be changed while in GS/T mode. Rotation of a frequency knob causes the NMs to bar and the frequency set to appear.

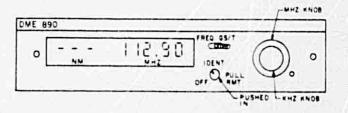
When locked-on to the set station the display immediately provides NMs and within 4 seconds KTs and MINs is presented.











2.7 POST INSTALLATION CHECK

Both the PreFlight check and Flight check are recommended after installation and major repair.

Use a Ramp Test Signal Generator or a local station of known distance.

- 1) Channel to proper frequency
- 2) Turn mode switch to GS/T
- 3) Distance (NM) should be in agreement with that set in the generator or that of the actual station (accuracy -.1 NM).
- 4) Check ground speed if using a generator.
- 5) Check that audio Ident tone is present.
- 6) If included in the installation, check the operation of Remote Channeling.

NOTE: Some Test Generators do not simulate actual signals and may not operate the Unit.

Flight

- 1) At 10,000 feet altitude, range 100 NM, check that there are no dropouts during a flat 360 turn.
- 2) At 6,000 feet altitude, range 50 NM, check that there are no dropouts during a flat 360 turn.
- 3) High Angle Check: While flying at a altitude of 6,000 to 10,000 feet (above the station's elevation) and from a distance of 10 NM, track inbound to the station and then track the reciprocal course. In each pass check the accuracy at the critical points... over the station and at the 10 NM point.
- 4) Orbit Approach: At a distance of 10 DME miles fly an orbit for one (1) minute. There shall be no dropouts. Repeat this flight in the opposite direction.
- 5) Electromagnetic Compatability: The DME should not cause the performance of other systems aboard the aircraft to be degraded nor should the DME be adversely affected by other onboard equipment. This can be checked by turning such equipments ON and OFF one by one and listening and viewing the resultant action. There should be no reactions.

2.8 LICENSE REQUIREMENTS

Operator:

The Federal Communications Commission requires that the operator of the transmitter in this equipment hold a Restricted Radio Telephone Operator Permit, or higher class license. A permit may be obtained by any U. S. citizen from the nearest field office of the FCC; no examination is required.

Aircraft:

The DME 890, as installed in the aircraft, requires an Aircraft Radio Station License. This license is obtained by filing FCC Form 404. The Unit may be operated for up to 30 days without a station license, after filing the FCC Form 404 and while awaiting receipt of the station license, providing a copy of the FCC Form 404 is kept in the aircraft. HOWEVER, if the aircraft has been previously licensed for a DME, resubmittal of FCC Form 404 is not required.

This equipment has been type accepted by the FCC and entered on their list of type accepted equipments as "NARCO DME 890".

CAUTION

The UHF transmitter in this equipment is guaranteed to meet Federal Communications Commission approval only when a NARCO crystal is used. The use of other than NARCO Crystals will void manufacturers warranty.

NARCO AVIONICS DME 890

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	VOR/DME CHANNEL PAIRING AND OPERATING FREQUENCIES

3.1 BASIC DME GROUND/AIRBORNE OPERATION

A full cycle of DME operation includes the transmission of a radio signal from the aircraft to the ground station and reply from the ground station to the aircraft. The time required for this process is determined by the distance between the aircraft and ground The aircraft transmits a pair of pulses at (approximately) a 30 Hz repetation rate and the signal is received at the ground station as shown in Figure 3-1. After a fixed delay of 50 microseconds (us) by the ground station, it transmits a pulse pair back to the aircraft. The airborn receiver must then confirm that: pulse pair is the result of its original transmission, measure the time taken for this round trip radio signal, and display the time period as distance in nautical miles. The airborne DME must take into consideration that the ground station simulates these events when not being interrogated. The ground station also takes time-out from replies to transmit its own identification (IDENT) that consists of regularly spaced pulses (dots and dashes of Morse code) that can be heard on the aircraft's audio system.

The DME is therefore an instrument that measures the time required for a radio signal to travel to and from the ground station. The time required is a function of the distance measured in nautical miles and the 50 us delay in the transmission of a reply. The radio wave requires 12.36 us to travel through one nautical mile of space and return. The DME has a resoultion of 0.1 nm. The 50 us delay by the ground station is to allow the DME receiver to recover from the DME transmitter blast. This 50 us delay is the same for all DME ground station transmitters. The airborne DME compensates for this 50 us delay. The DME is capable of recognizing the correct reply, although not every interrogation gets a reply.

The DME ground station has three basic functions: retransmits any receiver signal, during "off time", generates squitter, and generates an IDENT signal. When retransmitting, this ground station reply may be in response to an interrogation from another aircraft, the DME, however, is able to disregard the other replies, recognize only the correct reply and process only this signal. If the ground station is sending IDENT or squitter, or replying to another aircraft, it will not reply to your DME interrogations.

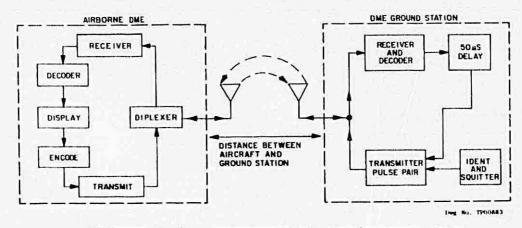


FIGURE 3-1. ELEMENTARY AIR/GROUND DME

3.2 DME 890 AIRBORNE OPERATION

The DME transmitter operates within the frequency range of 1041 through 1150 MHz and the receiver frequencies are 978 through 1213 MHz; transmit and receive frequencies on any given channel are offset by 63 MHz, the receiver IF frequency. These operating frequencies are paired to operate with the associated OMNI channel as shown in Table 3.1 The DME channel is selected by the setting of the DME's MHz and KHz channel select switches, or by a remote NAV Receiver if the DME's remote channeling capability is used. VOR channels 108.00 through 117.95 MHz are indicated as they are paired directly with the DME ground station located at VORTAC or VOR ground stations. The channeling lines which are ARINC 2-outof-5, are connected directly to the search track counters as shown in Figure 3-2. The synthesizer operating frequency is 1/2 the transmit output frequency. The pulse repetition frequency (PRF) source is the microprocessor that turns on the transmitter pulse modulator at approximately 30 Hz rate. The DME operates in a simultaneously displayed distance, velocity and time-to-station (TTS) mode, or a displayed frequency and distance.

TABLE 3.1. VOR/DME CHANNEL PAIRING AND OPERATING FREQUENCIES

Channel Number	Channel (MHz)	Interrogating Frequency (MHz)	VCO Frequency (MHz)	Airborne Interrogating Pulse Code (us)	Ground Reply Frequency (MHz)	Roply Pulse Spacing (us)	Channel Number	Channel	Interrogating Frequency (MHz)	VCO Prequency (MHz)	Airborne Interrogating Pulse Code (us)	Ground Reply Frequency (MHz)	Reply Pulse Spacing (us)
+17X	108.00	1041	520.50	12	978	12	35X	109.80	1059	529.50	12	996	12
17Y	108.05	1041	520.50	36	1104	30	35Y	109.85	1059	529.50	36	1122	30
18X	108,10	1042	521.00	12	979	12	36X	109.90	1060	530.00	12	997	12
18Y	108,15	1042	521.00	36	1105	30	36Y	109.95	1060	530.00	36	1123	30
19X	108,20	1043	521.50	12	980	12	37X	110.00	1061	530.50	12	998	12
19Y	108,25	1043	521.50	36	1106	30	37Y	110.05	1061	530.50	36	1124	30
20X	108.30	1044	522.00	12	981	12	38X	110.10	1062	531.00	12	999	12
20Y	108.35	1044	522.00	36	1107	30	38Y	110.15	1062	531.00	36	1125	30
21X	108.40	1045	522.50	12	982	12	39X	110.20	1063	531.50	12	1000	12
21Y	108.45	1045	522.50	36	1108	30	39Y	110.25	1063	531.50	36	1126	30
22X	108.50	1046	523.00	12	983	12	40X	110.30	1064	532.00	12	1001	12
22Y	108.55	1048	523.00	36	1109	30	40Y	110.35	1064	532.00	36	1127	30
23X	108.60	1047	523.50	12	984	12	41X	110,40	1065	532.50	12	1002	12
23Y	108.65	1047	523.50	36	1110	30	41Y	110,45	1065	532.50	36	1128	30
24X	108.70	1048	524.00	12	985	12	42X	110,50	1066	533.00	12	1003	12
24Y	108.75	1048	524.00	36	1111	30	42Y	110,55	1066	533.00	36	1129	30
25X	108.80	1049	524.50	12	986	12	43X	110.60	1067	533.50	12	1004	12
25Y	108.85	1049	524.50	36	1112	30	43Y	110.65	1067	533.50	36	1130	30
26X	108.90	1050	525,00	12	987	12	44X	110.70	1068	534.00	12	1005	12
26Y	108.95	1050	525,00	36	1113	30	44Y	110.76	1068	534.00	36	1131	30
27X	109.00	1051	525.50	12	988	12	45X	110,80	1069	534.50	12	1006	12
27Y	109.05	1051	525.50	36	1114	30	45Y	110,85	1069	534,50	36	1132	30
28X	109.10	1052	526,00	12	989	12	46X	110.90	1070	535.00	12	1007	12
28Y	109.15	1052	526.00	36	1115	30	46Y	110.95	1070	535.00	36	1133	30
29X	109.20	1053	526.50	12	990	12	47X	111.00	1071	535.50	12	1008	12
29Y	109.25	1053	526.50	36	1116	30	47Y	111.05	1071	535,50	36	1134	30
30X	109.30	1054	527.00	12	991	12	48X	111.10	1072	536.00	12	1009	12
30Y		1054	527.00	36	1117	30	48Y	111.15	1072	536.00	36	1135	30
31X	109.40	1055	527.50	12	992	12	49X	111.20	1073	536.50	12	1010	12
31Y		1055	527.50	36	1118	30	49Y	111.25	1073	536.50	36	1136	30
32X	109.50	1056	528.00	12	993	12	50X	111.30	1074	537.00	12	1011	12
32Y	109.55	1056	528.00	36	1119	30	50Y	111.35	1074	537.00	36	1137	30
33X	109.60	1057	528.50	12	994	12	51X	111.40	1075	537.50	12	1012	12
33Y	109.65	1057	528.50	36	1120	30	51Y	111.45	1075	537.50	36	1138	30
34X	109.70	1058	529.00	12	995	12	52X	111.50	1076	538.00	12	1013	12
34Y		1058	529.00	36	1121	30	52Y	111.55	1076	538.00	36	1139	30

Channel Number	Channel (MHz)	Interrogating Frequency (MHz)	vco Frequency (MHz)	Airborne Interrogating Pulse Code (us)	Ground Reply Frequency (MHz)	Reply Pulse Spacing (us)
53X	111.60	1077	538.50	12	1014	12
53Y	111.65	1077	538,50	36	1140	30
54X	111.70	1078	539.00	12	1015	12
54Y	111.75	1078	539.00	36	1141	30
55X	111.80	1079	539.50	12	1016	12
55Y	111.85	1079	539.50	36	1142	30
56X	111.90	1080	540.00	12	1017	12
56Y	111.95	1080	540.00	36	1143	30
57X	112.00	1081	540.50	12	1018	12
57Y	112.05	1081	540.50	36	1144	30
58X	112,10	1082	541.00	12	1019	12
58Y	112,15	1082	541.00	36	1145	30
59X	112.20	1083	541.50	12	1020	12
59Y	112.25	1083	541.50	36	1146	30
70X	112.30	1094	547.00	12	1157	12
••70Y	112.35	1094	547.00	36	1031	30
71X	112.40	1095	547.50	12	1158	12
••71Y	112.45	1095	547.50	36	1032	30
72X	112.50	1096	548,00	12	1159	12
••72Y	112.55	1096	548,00	36	1033	30
73X	112.60	1097	548.50	12	1160	12
••73Y	112.65	1097	548.50	36	1034	30
74X	112.70	1098	549.00	12	1161	12
••74Y	112.75	1098	549.00	36	1035	30
75X	112.80	1099	549,50	12	1162	12
••75Y	112.85	1099	549,50	36	1036	30
76X	112.90	1100	550.00	12	1163	12
••76Y	112.95	1100	550.00	36	1037	30
77X	113.00	1101	550.50	12	1164	12
••77Y	113.05	1101	550.50	36	1038	30
78X	113,10	1102	551.00	12	1165	12
••78Y	113,15	1102	551.00	36	1039	30
79X	113,20	1103	551.50	12	1166	12
••79	113,25	1103	551.50	36	1040	30
BOX	113.30	1104	552,00	12	1167	12
	113.35	1104	552,00	36	1041	30

Channel Number	Channel (MHz)	Interrogating Frequency (MHz)	VCO Frequency (MHz)	Airborne Interrogating Pulse Code (us)	Ground Reply Frequency (MHz)	Reply Pulse Spacing (us)
81X	113.40	1105	552,50	12	1168	12
81Y	113.45	1105	552,50	36	1042	30
82X	113.50	1106	553.00	12	1169	12
82Y	113.55	1106	553.00	36	1043	30
83X	113.60	1107	553.50	12	1170	12
83Y	113.65	1107	553.50	36	1044	30
84X	113.70	1108	554.00	12	1171	12
84Y	113.75	1108	554.00	36	1045	30
85X	113.80	1109	554.50	12	1172	12
85Y	113.85	1109	554.50	36	1046	30
86X	113.90	1110	555.00	12	1173	12
86Y	113.95	1110	555.00	36	1047	30
87X	114.00	1111	555.50	12	1174	12
87Y	114.05	1111	555.50	36	1048	30
88X	114.10	1112	556.00	12	1175	12
88Y	114.15	1112	556.00	36	1049	30
89X	114.20	1113	556.50	12	1176	12
89Y	114.25	1113	556.50	38	1050	30
90X	114.30	1114	557.00	12	1177	12
90Y	114.35	1114	557.00	36	1051	30
91X	114.40	1115	557.50	12	1178	12
91Y	114.45	1115	557.50	36	1052	30
92X	114.50	1116	558.00	12	1179	12
92Y	114.55	1116	558.00	36	1053	30
93X	114.60	1117	558.50	12	1180	12
93Y	114.65	1117	558.50	36	1054	30
94X	114.70	1118	559.00	12	1181	12
94Y	114.75	1118	559.00	36	1055	30
95X	114.80	1119	559.50	12	1182	12
95Y	114.85	1119	559.50	36	1056	30
96X	114.90	1120	560.00	12	1183	12
96Y	114.95	1120	560.00	36	1057	30
97X	115.00	1121	560.50	12	1184	12
97Y	115.05	1121	560.50	36	1058	30
98X	115.10	1122	561.00	12	1185	12
98Y	115.15	1122	561.00	36	1059	30

TABLE 3.1. Continued

Channel Number	Channel (MHz)	Interrogating Frequency (MHz)	VCO Frequency (Miz)	Airborne Interrogating Pulse Code (us)	Ground Reply Frequency (MHz)	Reply Pulse Spacing (us)
99X	115.20	1123	561.50	12	1186	12
99Y	115.25	1123	561.50	36	1060	30
100X	115.30	1124	562.00	12	1187	12
100Y	115.35	1124	562.00	36	1061	30
101X	115,40	1125	562.50	12	1188	12
101Y	115,45	1125	562.50	36	1062	30
102X	115,50	1126	563.00	12	1189	12
102Y	115,55	1126	563.00	36	1063	30
103X	115,60	1127	563,50	12	1190	12
103Y	115,65	1127	563,50	36	1064	30
104X	115.70	1128	564.00	12	1191	12
104Y	115.75	1128	564.00	36	1065	30
105X	115.80	1129	564.50	12	1192	12
105Y	115.85	1129	564.50	36	1066	30
106X	115.90	1130	565,00	12	1193	12
106Y	115.95	1130	565,00	36	1067	30
107X	116.00	1131	565,50	12	1194	12
107Y	116.05	1131	565,50	36	1068	30
108X	116,10	1132	566,00	12	1195	12
108Y	116,15	1132	566,00	36	1069	30
109X	116,20	1133	566,50	12	1196	12
109Y	116,25	1133	566,50	36	1070	30
110X	116.30	1134	567.00	12	1197	12
110Y	116.35	1134	567.00	36	1071	30
111X	116,40	1135	567,50	12	1198	12
111Y	116,45	1135	567,50	36	1072	30
112X	116.50	1136	568,00	12	1199	12
112Y	116.55	1136	568,00	36	1073	30
113X	116.60	1137	568,50	12	1200	12
113Y	116.65	1137	568,50	36	1074	30
114X	116,70	1138	569,00	12	1201	12
114Y	116,75	1138	569,00	36	1075	30
115X	116.80	1139	569,50	12	1202	12
115Y	116.85	1139	569,50	36	1076	30
116X	116,90	1140	570.00	12	1203	12
116Y	116,95	1140	570.00	36	1077	30

Channel Number	Channel (MHz)	Interrogating Frequency (MHz)	VCO Frequency (MIIz)	Airborne Interrogating Pulse Code (us)	Ground Heply Frequency (MHz)	Reply Pulse Spacing (us)
117X	117.00	1141	570.50	12	1204	12
117Y	117.05	1141	570.50	36	1078	30
118X	117.10	1142	571.00	12	1205	12
118Y	117.15	1142	571.00	36	1079	30
119X	117.20	1143	571,50	12	1206	12
119Y	117.25	1143	571,50	36	1080	30
120X	117.30	1144	572.00	12	1207	12
120Y	117.35	1144	572.00	36	1081	30
121X	117,40	1145	572,50	12	1208	12
121Y	117,45	1145	572,50	36	1082	30
122X	117.50	1146	573.00	12	1209	12
122Y	117.55	1146	573.00	36	1083	30
123X	117,60	1147	573.50	12	1210	12
123Y	117,65	1147	573.50	36	1084	30
124X	117.70	1148	574,00	12	1211	12
••124Y	117.75	1148	574,00	36	1085	30
125X	117.80	1149	574.50	12	1212	12
••125Y	117.85	1149	574.50	36	1086	30
126X	117.90	1150	575.00	12	1213	12
••126Y	115.95	1150	575.00	36	1087	30

TABLE 3.2. X/Y MODES FREQUENCY CORRELATION SUMMARY

VHF Channel Number	Frequency (MHz)	DME Op Receive	eration Transmit	LO Frequency 3 X Synth, freq.
108.0 TO 112.2 (0.1 MHz)	978 TO 1020	x		Above receiver
108,0 TO 112,2	1041 TO 1083		x	frequency (receiv.r freq. +63)
112,3 TO 117,9 (0,1 WHz)	1094 TO 1150		x	Below receiver
112.3 TO 117.9	1157 TO 1213	x		frequency (receiver freq63)
108.05 TO 112.25	1041 TO 1083		¥	Below receiver
113,35 TO 117,55	1104 TO 1146	Y		frequency (receiver freq63)
112,35 TO 117,95	1094 TO 1150		Y	Above receiver
112,35 TO 117.95	1031 TO 1087	Y		frequency (receiver freq. +63)

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Spacing between pulse pairs

X = 12 microsec (0.1 MHz Channels)------Both Y = 38 microsec (0.05 MHz Channels)--Air to Ground Y = 30 microsec (0.05 MHz Channels)--Ground to Air

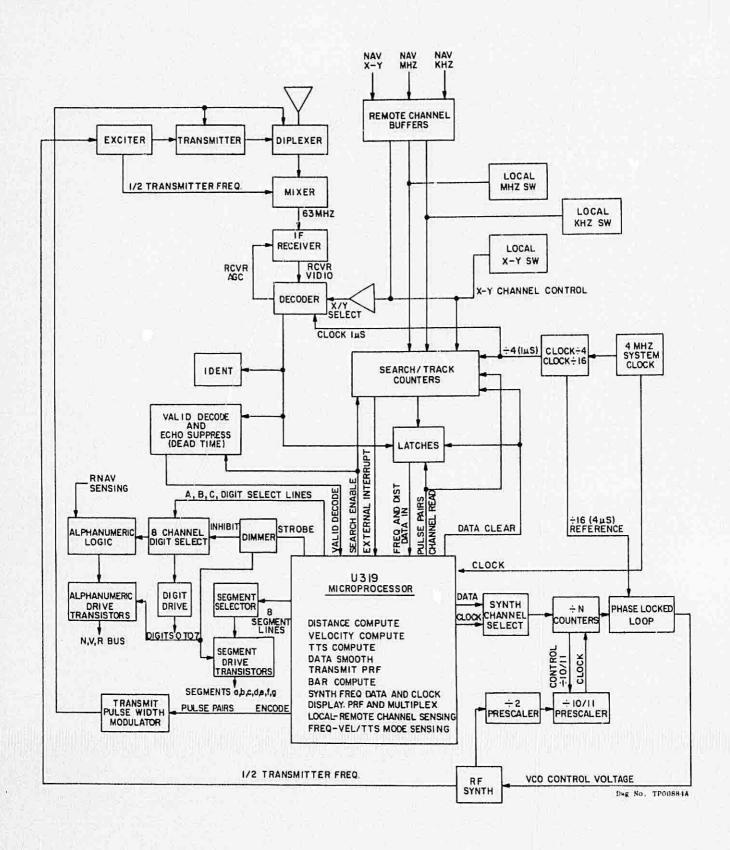


FIGURE 3-2. DME 890 FUNCTIONAL BLOCK DIAGRAM

3.3 OPERATION IN THE GS/T MODE (NM, KT, MIN)

The distance/velocity/time-to-station (GS/T) will be described using Figure 3-2 as a guide. (GS/T also referred to as ground speed/time).

When the mode switch on the front panel is placed in the GS/T position the information displayed will be Distance to station (nautical miles), Velocity (nautical miles per hour) and Time-to-Station in minutes. All are displayed simultaneously.

The transmitter is turned on as follows: The microprocessor (U319) generates pairs of pulses, 12 or 36 microseconds (us), at a PRF of These pulse pairs are present at the "Encode" port of the microprocessor and act as reset pulses for the decoder and as trigger pulses for the transmit pulse width modulator. The pulse pair from the modulator turns on the transmitter. The Exciter stage of the transmitter runs continuously, whereas the first and final pulse stages and the Diplexer of the transmitter are turned on by the pair of 50V pulses from the Modulator. The Diplexer connects either the receiver or transmitter to a single antenna and protects the receiver from damage due to overload when the transmitter The RF output from the antenna is pairs of pulses of RF energy at a selected frequency between 1041 and 1150 MHz. The pulses are 3.5 us wide having 12 us spacing on 0.1 MHz ("X" channels) and 36 us spacing on 0.05 MHz ("Y" channels). The synthesizer which operates at 1/2 the transmitter frequency, is injected into the Exciter section of the transmitter. The second buffer stage of the Exciter injects the 1/2 frequency into the Mixer where it is doubled and mixed with the incoming reply signal to give a 63 MHz IF that is now injected into the Receiver. Example: when the selected channel is 108.00, the transmit frequency is 1041 MHz, the synthesizer (Exciter) output is 520.5 MHz, and the receiver frequency 978 MHz. The received pulse pair (978 MHz) and Exciter frequency 520.5 MHz are combined in the mixer where the Exciter frequency is doubled (2 X 520.5 = 1041 MHz) and heterodyned with the received frequency of 978 MHz (1041 - 978 = 63 MHz). The pulse pairs are repeated at a 30 Hz rate. Approximately 50 us (equal to the ground station fixed delay) after the second pulse from the modulator turns on the transmitter, the microprocessor's search enable port enables the Dead Time Multivibrator, and turns on the search track counters. Now 1 us clock pulses feed three search track counters whose terminal count is 2048 us. The 1 us clock corresponds to the time required for the transmitted signal to travel 0.1 of a nautical mile and return. During the period that the Receiver is awaiting a reply from the ground station, the search track counters are measuring the time as they are being loaded with a train of clock pulses, one pulse for each 0.1 nautical mile to the ground station. With the modulation pulses removed from the Diplexer, the Receiver awaits the pulse pair reply from the ground station.

3.3 Continued

This 63 MHz IF frequency is amplified, detected, and converted to a logic level and fed to the Decoder. The Decoder confirms that the pulses of the received pulse pair are separated by the desired The decoded reply is used as a clock pulse interval (12 or 30 us). to transfer the accumulated count (present at the output of the Search Track Counters at the time of the received reply) into a latch. The microprocessor will accept this data only if the "Valid Decode" port goes logic low at the time of data from the latch The "Valid Decode" line is controlled by a Dead Time Multivibrator which is triggered by the decoded reply pulse. The Dead Time is approximately 60 us. Upon the initial trigger of this multivibrator, the microprocessor accepts the Search Track Counter Data, but during the 60 us Dead Time, any received decoded replies are ignored by the microprocessor. This Dead Time is used as an "Echo Suppression" (Signal Multipath), by holding off the decoder.

The microprocessor now compares this valid data with the valid data from a previous interrogation, if occurring at a synchronous rate, the microprocessor will do the following: compute the time between valid data which is equivalent to DME distance to ground station, compute the rate of change of distance with time which is velocity, and compute the time-to-station by calculating T= Distance + Velocity. The displayed information of Velocity and Time are accurate only when flying directly to or from the station. When the Search Track Counters are started, they count through to the terminal count of The decoded reply does not stop the counters, only the instantanious condition of the counters is sampled and stored. The microprocessor encodes the digit and segment lines used to illuminate the Display on the front panel. If there are no valid decoded replies for approximately 10 seconds the panel Display will signal a fault by displaying "bars" in place of the numerical distance display. This signifies to the pilot there is no accurate or useful information received by the DME.

During the Ground Speed/Time (GS/T) mode of operation, the microprocessor samples the frequency control lines at a 30 Hz rate but does not normally display this information, however, if there is a loss of signal either permanently or temporarily (greater than 10 seconds) the distance section of the display will show "bars" and the frequency the set is tuned to will be displayed in place of the velocity and time-to-station. Also, if the pilot changes the frequency, the distance will bar and the selected frequency will appear temporarily until the DME "locks on" at the new frequency and approximately 4 seconds later the display reverts back to its previous presentation.

3.4 OPERATION IN FREQUENCY MODE (MHz)

In the Frequency mode, the DME continues to operate as in the distance mode, however, only distance and frequency information are displayed. The microprocessor senses that the mode switch is in a frequency position and encodes the proper alphanumeric, digit and segment lines of the display to present only distance and frequency.

3.5 REMOTE CHANNEL OPERATION

The DME 890 has a built-in capability of being remotely channeled by those NAV receivers whose remote channeling lines conform to the ARINC (2/5) Code. The "Remote" switch is located on the front panel and is pulled to activate, at that time the letters "RMT" appear on the display to alert the pilot that the DME is in Remote Mode. The DME's frequency select switches are also rendered inactive and the remote channeling buffers are activated, coupling the frequency control lines to the remote NAV Receiver. If the "Remote" switch is activated when there is no actual remote NAV Receiver connected to the DME 890, the microprocessor, which has sensed that the Remote switch has been activated, will print the word "Error" in the numerical part of the display and cause the display to flash at a 3 Hz rate.

3.6 AREA NAVIGATION MODE (RNAV)

The DME 890 has area navigation (RNAV) capability, but only with a future NARCO designed RNAV. There are four input/output lines consisting of: RNAV Mode Control, RNAV data out, RNAV data in, and RNAV clock out. When the RNAV Mode Control line goes to logic low, the following events will occur: the letters "RNAV" will appear in the display alerting the pilot that the DME is in RNAV Mode, the microprocessor will send a serial clock and serial data (distance to VORTAC) to the RNAV, and accept serial input data (computed distance to the waypoint) from the RNAV. The distance displayed will be nautical miles to the RNAV WAYPOINT.

3.7 GENERAL

This circuit description supports the search track counters and the associated components necessary to present the microprocessor with valid information so it can compute the distance, velocity and time-to-station. Subsequent subsections separate these components and describe their operation in detail.

3.7.1 Microprocessor Cycle of Operation

To facilitate the understanding of a Search Track Epic *, a routine the microprocessor follows will be described. Figure 3.3 is used as a guide.

- 1. The cycle begins with the microprocessor "Encode" port sending 12 or 36 us pulse pairs to the transmit modulator to turn on the transmitter.
- 2. 53 us later (this time is measured from the leading edge of the search the second encode pulse to the leading edge of the search enable pulse) the "Search Enable" line enables the Search Track counters for the terminal count (0-160 miles) of 2048 us. During the microprocessor's cycle of operation there will be a total of 15 terminal counts, however, it is only during the first terminal count, known as the "Search Track Epic", that valid information can be received in response to the transmission that occured 53 us prior to the beginning of the search track epic. The search enable line also enables the Dead Time multivibrator.
- 3. Concurrent with the search enable line, the "data clear" line is encoded and releases the latches and Search Track counters from their reset state. This line is active logic high for the Terminal Count.
- 4. At the termination of the count (2048 us), a pulse, EXT. INT. (external interrupt), is sent to the microprocessor. This pulse is used by the microprocessor in two ways:
 - a. To signal the microprocessor to encode the digit and segment lines for the display.
 - b. As a clock to limit the number of external interrupt pulses to 15, at which time the microprocessor will take time out to do math calculations, read the ground station squitter which will be used to establish the transmitter PRF, and set up the Channel Read pulse pairs and the Encode pulse pairs.
- * A Search Track Epic is defined as a transmission from the DME to the ground station, the reception and decoding of the ground stations reply transmission, an on-the-fly sampling of the Search Track counters elasped time between transmission and reply, and the end of the 0-160 mile count (Terminal).

3.7.1 Continued

5. The cycle ends with the microprocessor generating a pair of "Channel Read" pulses which are used to sample the frequency control lines.

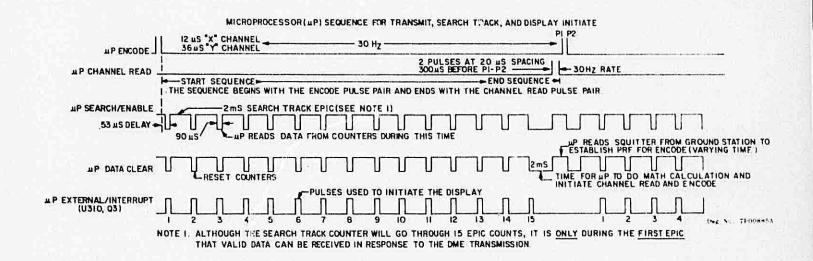


FIGURE 3-3. MICROPROCESSOR

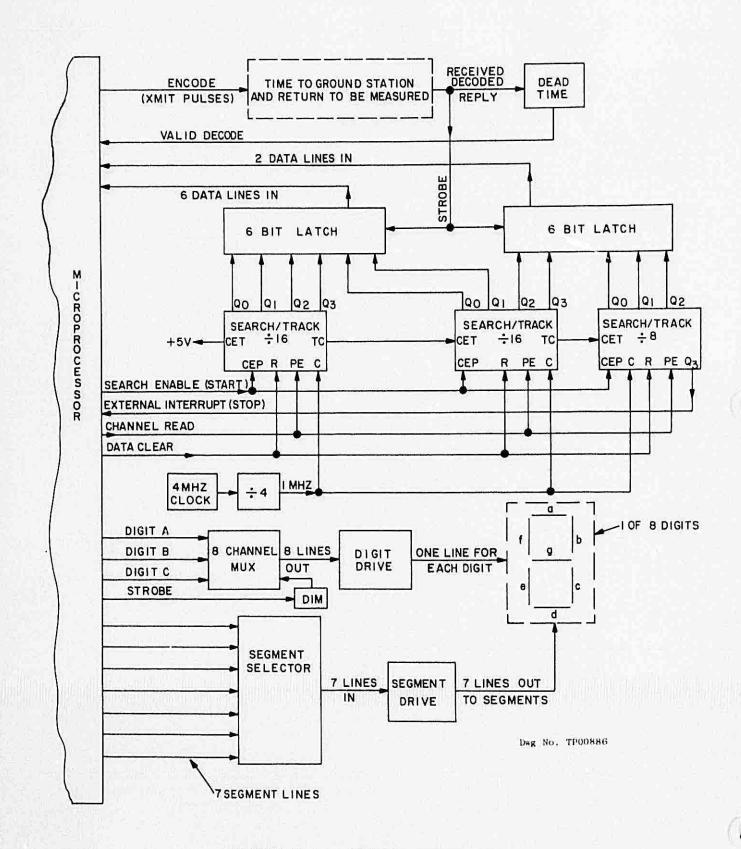


FIGURE 3-4. SEARCH TRACK EPIC

3.7.2 Search Track Epic

The front panel display includes 8 digits and the extreme left digit never increases beyond "1". The display is the result of the valid data acquired from the ÷2048 search track counters during the search track epic. The capability of the display is considered to be 160 nautical miles. For the purpose of an explaination, one complete Search Track Epic will be described showing the method of data acquisition, the starting and stopping of the counters, and the display of the digits. The mode switch on the front panel is assumed to be in the GS/T position. (Refer to Figures 3-3, 3-4, 3-5)

During actual operation, the display is in increments of 0.1 nautical mile. The Search Track Counters count increments of 1.0 microseconds obtained from the divided down (÷4) crystal controlled 4 MHz clock. The counters are started by the "Search Enable" port from the microprocessor 53 us after the "encode" port has turned on the transmitter. The 1 MHz clock pulses are fed into the counters without interruption. A single Search Track counter consists of four edge triggered "D" flip-flops (F-F) in series, capable of 16 counts with an output line from the output of each of the four flip-The counters output is in a binary format. Each of the four output lines is capable of indicating the logic state of its associated F-F, a "1" (high) or "0" (low). Also there is a Terminal Count (TC) output line which is fully decoded and is high only on the 15th count and returns to logic low on the 16th count. The TC output from the first counter is connected to the "Count Enable Trickel" (CET) input of the second counter, and the TC output of the second counter is connected to the CET input of the third The Count Enable Trickle input must be logic high to enable the counter. A logic low at the CET input inhibits the count sequence and freezes the output lines in their existing states at the time the CET input goes logic low. The condition of each output line is shown in Figure 3-5.

To satisfy these operating conditions, apply the control signals to the Search Track Counters. The "data clear" line from the microprocessor has set all the counters and latches to their zero state (all four output lines are logic low). The uninterrupted 1 MHz clock is present at the clock input of the counters. The "search enable" line from the microprocessor goes to logic high, enabling the counters. As the clock pulses are loaded into the counter, the count progresses in a binary sequence as shown in Figure 3-5 and Table 3.3.

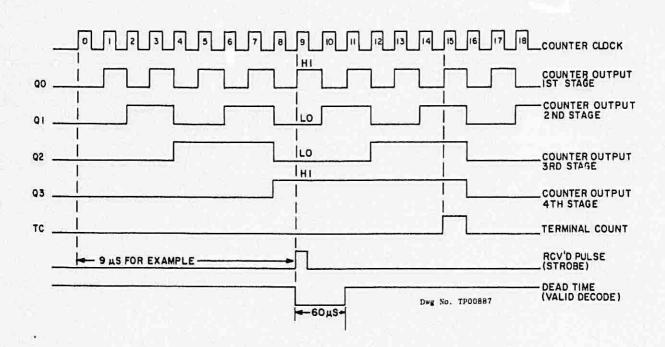


FIGURE 3-5. SEARCH TRACK TIMING DIAGRAM

TABLE 3.3. 4 BIT BINARY COUNTER

COUNT			UTPUT	
	Qo	Q1	Q2	Q3
Reset 0	L	L	L	L
1	Н	L	L	L
2	L	н	L	L
3	H	н	L	L
4	L	L	Н	L
5	Н	L	н	L
6	L	Н	Н	L
7	Н	Н	Н	L
8	L	L	L	Н
9	H	L	L	Н
10	L	н	L	Н
11	Н	н	L	Н
12	L	L	H	Н
13	Н	L	Н	Н
14	L	H	Н	Н
15	н	Н	Н	Н
16	L	L	L	L

L= Low H=High

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3.7.2 Continued

If, at the count of 9, a reply strobe pulse is fed into the 6 bit latches, as shown in Figure 3-4 and Figure 3-5, the data at the latch inputs (Q0/Q3 are high, Q1/Q2 are low) will be transferred to the latch outputs for the microprocessor to read. At the same time the latches are being strobed, the "Dead Time" multivibrator is triggered (60 us), and its output is the "Valid Decode" input to the microprocessor. Upon receipt of the Valid Decode, the microprocessor accepts the data from the latches and during the 60 microsecond duration of the multivibrator it will not accept any new data. This 60 us Dead Time is to suppress echoes (signal multipath).

The counter continues the count sequence and upon reaching the 15th count the Terminal Count (TC) line goes logic high and enables the next counter. On the 16th count, the Q0 output of the 2nd counter changes state, and the TC line of the first counter goes logic low and freezes the 2nd counter while the 1st counter again starts its count sequence. Thus it can be seen that the 2nd counter is being enabled on by only 1-out-of-16 pulses so that in order to reach its terminal count of 16, there must be a total of 256 pulses (16 X 16). The 3rd counter needs 2048 pulses (256 X 8) in order for its Q3 output line to go high on its count of 8. This Q3 output from the 3rd counter is fed to the "External Interrupt" (EXT. INT.) port of the microprocessor and is used by the microprocessor in two principle ways:

1. As a command to light the display.

2. As a clock to limit the number of external interrupt pulses to 15.

At the conclusion of the Epic, the "data clear" and "search enable" lines go logic low to clear the counters and shut them down. After a period of approximately 90 us, the two lines go logic high to start another count. The microprocessor will initate fifteen more terminal counts and at the conclusion of the 16th terminal count (see Figure 3-3), will shut down the Search Track counters for approximately 1 ms. During this off period, the microprocessor is doing math calculations and setting up the sequence of reading ground station squitter, initiating channel read and encode pulse pairs. At the conclusion of the 1 ms shutdown, the microprocessor starts the Search Track Counters and samples the ground station squitter which it will use to establish the "Encode" PRF rate. Next, the microprocessor shuts down and clears the Search Track Counters and then issues a "channel read" command consisting of 2 pulses. The first pulse will load the frequency control lines data into the Search Track Counters and upon receipt of the next Search Track Counter 1 MHz clock pulse, transfers this data to the inputs of the 6 bit latches. The 2nd "channel read" pulse strobes the 6 bit latches and transfers this data into the microprocessor where it is compared to the previous "Channel Read" data. As was stated previously, the mode switch is in the GS/T position.

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3.7.2 Continued

During the "Channel Read" command, the microprocessor reads the "EXT. INT." line to sense which frequency mode the pilot has selected. If the EXT. INT. line is logic high, the mode switch is in the "FREQ" position whereas a logic low indicates the GS/T position. In the GS/T mode, the display is Distance, Velocity, and Time-to-Station. When the microprocessor compares the current data with the previous data and they agree, no change will occur in the display. However, if the data does not agree because the pilot has selected a new frequency, then the microprocessor will initiate the following action:

- 1. Encode the synthesizer channel data and clock lines to update the synthesizer frequency. This occurs only once.
- 2. Cause "bars" to appear in the distance section of the display.
- 3. Temporarily display the new frequency selected. When the DME locks on to the new station approximately 4 seconds later, the display will automatically revert back and read Distance, Velocity, and Time-to-Station.

Upon receipt of each EXT. INT. pulse at the end of each terminal count the microprocessor will send a "strobe" pulse to the display "DIMMER MULTIVIBRATOR" and encode the digit and segment lines to light the display. The digits are not lighted in sequence (i.e. 0, 1, 2, 3, ---- 7), rather they are selected in a specific sequence to prevent a possible ripple effect that may be seen by the human eye. The digits and segments are strobed for approximately 2 ms each at a 60 Hz rate.

3.8 DETAILED CIRCUIT DESCRIPTION

3.8.1 Modulator

The Modulator turns on the transmitter when directed to by the Encode port of the microprocessor (U319). The Modulator is separated into a pulse width control section and a driver section as shown in Figure 3-6. The Encode port triggers the pulse width multivibrator (U316) at a PRF of 30 Hz with a pair of pulses whose spacings are 12 microseconds (us) (X channel), or 36 us (Y channel). The period of U316 is adjusted by R356 to set the width of the transmitter's output pulses to 3.5 us.

The modulator driver receives +60 volts from the power supply and Zener diode, CR323, regulates this at 51V. This 51V is the supply voltage for the transmitter and Modulator drive transistor, Q301. In the quiescent state, the base of Q301 is clamped one diode junction above the 51V Zener voltage and is sitting at 51.7V. Clamp diode, CR324, prevents the base/emitter voltage of Q301 from exceeding its rated reverse breakdown of 5V. When U316 is triggered, its Q2 (pin 5) and $\bar{Q}2$ (pin 12) outputs turn on Q302. Q302 pulls the base voltage at Q301 down, thereby turning on Q301. Q301's collector rises to 50V for a period of 3.5 us for each trigger pulse. (These pulses are used to modulate Q206, the pedestal modulator, in the Exciter section of the transmitter and Q103, the final transmitter modulator).

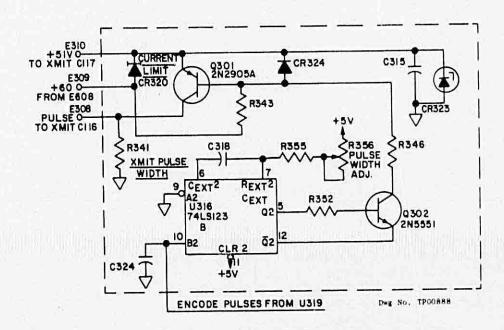


FIGURE 3-6. TRANSMIT PULSE MODULATOR

3.8.2 Transmitter

The Transmitter amplifies the RF excitation from the Synthesizer and doubles it's frequency when pulsed by the Modulator. The transmitter comprises 4 basic functional areas as shown in Figure 3-7, CW amplifiers Q201, Q202, Q203, and Q204, first pulse amplifier Q205, frequency doubler Q101, and final amplifier Q102. When provided with an excitation level of +3 dBm at 550 MHz, the exciter output frequency range is from 520.5 through 575 MHz and the transmitter output from 1041 to 1150 MHz, however, to simplify this description, the input and output frequencies will be 550 and 1100 MHz respectivily.

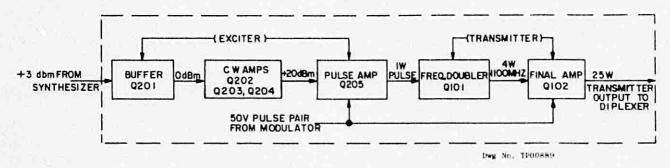


FIGURE 3-7. RF TRANSMITTER FUNCTIONAL BLOCK DIAGRAM

3.8.2.1 Exciter (low level RF amplifier) Refer to Schematic Fig. 6-2

The Exciter is a 5 transistor RF amplifier that provides 1 watt (+30 dBm) of pulsed drive to the frequency doubler, Q101. A resistive attenuator (R201, R202, R203) provides isolation between transmitter and synthesizer. C301 is the coupling capacitor to the input buffer stage, Q201. Q201's output is RC coupled to Q202, Q203, Q204, Q205, Q101, Q102. These capacitors, together with inductors L201, L202, L204, and L206 form the interstage matching networks. L207 and L101 are RF chokes.

Functionally, the Q202/Q203, Q203/Q204, and Q204/Q205 interstage coupling are identical. Each output stage uses a pair of capacitors as a divider network with one of the capacitors being adjustable so as to match the impedance between stages for maximum transfer of power. The output of Q202 is delivered to a special 50 ohm power splitter, T201, whose purpose is to split the signal into two paths, one going to the mixer at a 0 dBm level, and the other to Q203 at the same 0 dBm level. Q203 delivers a +10 dBm level to Q204 and Q204 delivers +20 dBm level to Q205. Part of the interstage coupling network between Q205 and the frequency doubler Q101 is a coaxial cable (Z201) cut to 1/4 wavelength which transforms the high impedance required at Q205's output, to a low impedance at Q101's input. This type of matching is necessary because the impedance looking into the emitter of Q101 is very low. L207 acts as a DC return for the emitter of Q101 and C221 is used to parallel the inductive component of the input impedance of Q101.



3.8.2.1 Continued

Separate decoupling circuits are used in Q202 and Q203 stages. C206 and C211 are used for RF bypass and R210 and R218 are used for decoupling from the +14 volt power supply.

All 5 stages of the Exciter receive base bias through voltage dividers (i.e. Q201 uses R206 and R205), and operate as Class A amplifiers. However, with no DC bias, Q101 and Q102 operate as Class C amplifiers. Upon receipt of a pair of 50 volt pulses from the pulse modulator, the pedestal modulator transistor, Q206, is turned on. These 50 volt pulses are Zener regulated down to 33 volts by CR201. The 550 MHz RF is continuously applied to Q205's input, when the 33 volt pulses are applied to the collector, the RF is gated on and this output is applied to the transmitter frequency doubler, Q101. The drive into Q101 is 1 watt of pulsed power.

3.8.2.2 Transmitter Doubler and Final Amplifier

The negative excursions of the pulsed RF applied to the emitter of Q101 turn this frequency doubler on. The 550 MHz is half-wave rectified, and according to theory, contains all the discrete numbered multiples (i.e. 1-2-3-4----) of the fundamental applied frequency, 550 MHz. At the collector of Q101 is a 1/4 wavelength, open coaxial cable (Z101) that acts as a RF short to the 550 MHz and as a high impedance to the 2nd harmonic, 1100 MHz. The power developed at the collector of Q101 is 4 watts and is coupled into the final amplifier, Q102. The impedance matching network coupling Q101 and Q102 consists of etched printed circuit transmission lines with adjustable capacitors, C102 and C118, providing the means for making an optimun match.

At the same time the pedestal modulator transistor (Q206) is turned on, the final amplifier modulator (Q103) is also turned on, however, the combination of R104 and L102 form a delay network to insure that the pulsed RF energy from Q101 will arrive at Q102 before Q102 is gated on. The reason for this is to insure that the final transmitted pulse pair will have the correct shape. The purpose of L107 at the emitter of Q103 is to provide a DC return path. The output from Q102 is 25 watts of pulse power. This is coupled through etched printed circuit transmission lines to the Diplexer.

3.8.3 Diplexer Receiver and AGC Circuits

Shown in Figure 3-8 are the receiver circuits in block form. RF energy is routed to the Band Pass Filter (BPF) by the Diplexer. BPF output energy is amplified by the RF amplifier and then mixed with the local oscillator signal from the power splitter T201, to produce a 63 MHz IF signal. This signal is then amplified in the receiver's 63 MHz IF amplifier, video detected, amplified and clipped to a 5 volt logic level and then sent to the Decoder.

The Decoder delays the video data for 12 microseconds (us) on X channels or 30 us on Y channels. Properly spaced pulse pairs will result in delayed data from the Decoder, and Video data to the Decoder, arriving coincidently at U313's AND gate inputs. A pulse from the AND gate will then enable the Sample and Hold AGC circuit that will then sample the Video amplifier's pulse amplitude and produce an AGC voltage for the 63 MHz IF circuits.

3.8.3.1 Diplexer and Band Pass Filter

The Diplexer alternately connects the antenna to the receiver or the transmitter as directed by the 33 volt pedestal modulator pulse pair. In the transmit mode, the positive going pedestal pulses will forward bias PIN diodes CR102 and CR103. Diode CR102 connects the transmitter output, through C106, to the antenna while CR103 is tapped to an etched printed circuit transmission line at the 1/4 wavelength point resulting in a high impedance to the transmitted frequencies.

This provides the necessary isolation between the transmitter and receiver. The purpose of L108 and C119 is to parallel resonate with the parasitic capacity of PIN diode, CR102. The purpose of C110 is to series resonate with the inductive component of PIN diode CR103. Inductor L103 is the DC return path for the diodes.

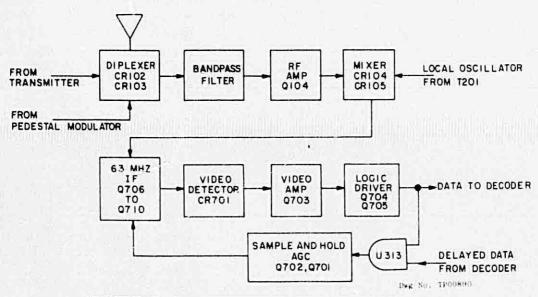


FIGURE 3-8. RECEIVER BLOCK DIAGRAM

3.8.3.2 RF Amplifier and Mixer

The RF amplifier consists of a low noise UHF transistor, Q104, stage which provides a gain of 8 dB over the frequency range of 978 to 1213 MHz. In addition to increasing the level of the incoming RF signal, it also acts as a isolation to the local oscillator signal in the mixer, preventing CW antenna radiation. L104 parallel resonates the parasitic capacity of Q104 and C113 couples the received signal into the mixer.

The local oscillator (LO) injection, which is 1/2 the frequency of the the transmitter, is coupled into the mixer through the series resonant combination of C114 and L105. The harmonics generated in the mixer will be isolated from the Exciter as this series L and C is seen as a high impedance to these frequencies. Mixing occurs in diodes CR104 and CR105 where the LO and Receiver RF signals are heterodyned, the 2nd harmonic of the LO with the received frequency provides a difference frequency of 63 MHz. The inductor L106 is a low impedance to 63 MHz and passes this signal to the IF Amplifier, however, its impedance to higher frequencies effectively isolates them from the IF Amplifier.

3.8.3.3 IF Amplifier and Detector (Refer to Figure 6-5)

The five stage IF amplifier, Q706 thru Q710, is comprised of a 63 MHz 6 pole filter consisting of 3 double-tuned interstage networks and a single tuned coil, L701. AGC voltage is applied to each of the IF transistors with the gain being proportional to the amount of AGC voltage available to supply base current to each transistor. The +14 volt supply to each collector is RF bypassed by a 1000 pF capacitor and decoupled by a 100 ohm resistor.

The 63 MHz energy from the Mixer is amplified and filtered by Q708, Q709, Q710, and further amplified by the two stage amplifier, Q706 and Q707. The signal at the collector of Q706 is coupled into a series resonant combination consisting of C708 and L701. This combination is broadly resonant at 63 MHz and the amplitude of the signal across L701 is greater than that across C708. This RF signal must now be video detected which is the purpose of Schottky diode, CR701. In addition to resonating with C708, L701 is the DC return for CR701.

The signal to be detected consists of two 3.5 microsecond (us) Gaussian bursts of 63 MHz energy. The negative excursion of the signal turns on CR701 and charges C702. The RC time constant of R702 and C702 is slightly greater than 3.5 us and far greater than the time of one cycle of 63 MHz. Thus when CR701 is initially turned on, C702 receives a negative charge, then, during the positive excursion the RF signal back biases CR701. C702 does not have enough time to recover its positive charge and C702 remains negative until the signal ends and C702 regains its positive potential. Therefore, the detection process is the formation of a negative pulse at C705 whose width is equal to the 3.5 us burst.

The purpose of L702 is to block 63 MHz energy from the Video Amplifier.

3.8.3.4 Video Amplifier and Logic Driver (Refer to Figure 6-5)

Video amplifier, Q703 is normally biased on, thus operating Class A, while logic drivers Q704 and Q705 are biased off. The gain of Q703 is approximately 200 which increases the detected video pulse amplitude to about 1 volt peak-to-peak. The negative detected pulse at C705 reduces the base current in Q703 generating a positive pulse at it's collector turning Q704 on. As Q704 turns on, its collector goes negative with respect to the emitter of PNP Q705 and turns on Q705 pulling the junction of R708 and R711 up to 7 volts.

This squared pair of 7 volt peak-to-peak pulses is of correct logic level to drive the decoder, U306. Diode CR702 clamps to ground any negative pulses, which would interfere with the AGC Sample and Hold circuitry.

3.8.3.5 Sample and Hold AGC (Refer to Figure 6-2 and Figure 6-5)

The Sample and Hold AGC controls the IF gain to produce uniform amplitude pulses at the output of the Video amplifier. In addition, only properly spaced pulses will enable AGC action. Proper pulse spacing is determined by AND gate U313. The receiver video pulses are applied to U306, the Decoder, and U313. The Decoder delays the receiver video pulses 12 us on X channels or 30 us on Y channels. Delayed data from the Decoder is applied to U313. If properly spaced, the second Video pulse from the receiver will occur coincident with the delayed first video pulse from the Decoder thereby generating a single pulse at the output of U313. This pulse will turn on Q702, and as a result, video pulses from the voltage divider R704 and R709 are gated from the collector of Q702 to the emitter and charged up holding capacitor C703. These sampled video pulses cause Q701 to conduct. Normally, transistors Q708 thru Q710 receive bias from the +14 volt supply which is divided down by R701 and each 470K base resistor (R714, R717, R720, R723, R726). When video pulses turn on Q701, the AGC voltage is reduced according to the amplitude of these pulses. Therefore, the gain of the IF stages is automatically controlled.

3.8.4 Decoder

3.8.4.1 General

The purpose of the Decoder is to examine the received signals for proper pulse spacing (i.e. either 12 or 30 us). Incorrectly spaced pulse pairs are rejected while correctly spaced pulse pairs are accepted and routed to the IDENT multivibrator, Receiver AGC circuitry, and Dead Time multivibrator.

3.8.4.2 Theory (Refer to Figure 3-9 and Figure 6-2)

The Decoder is comprised of a shift register (delay line) U306, Coincident AND gate U313D, and X-Y channel select inverter U314A as shown in Figure 3-9. The shift register functions as a digital delay line operating in a serial-in/serial-out mode with clock pulses shifting the data at a 1 microsecond rate. The length (delay) may be programmed to any number of bits between 1 and 64 by applying the proper logic 1 (high) or logic 0 (low) to the control inputs (L1, L2, L4, L8, L16, L32). (See Table 3.4)

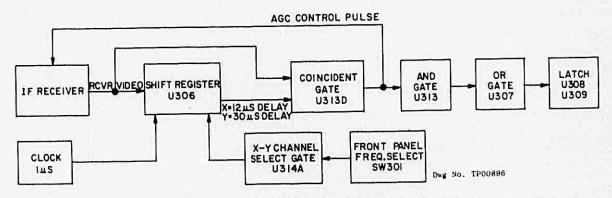


FIGURE 3-9. DECODER BLOCK DIAGRAM

TABLE 3.4. U306 PROGRAM

CHANN	REGISTER LENGTH	CONTROL IMPUTS					
	MICROSECONDS	L1	L2	L4	L8	L16	L32
x	12	0	0	1	1	0	0
Y	30	0	1	1	1	1	0

Dwg. No. TP00880

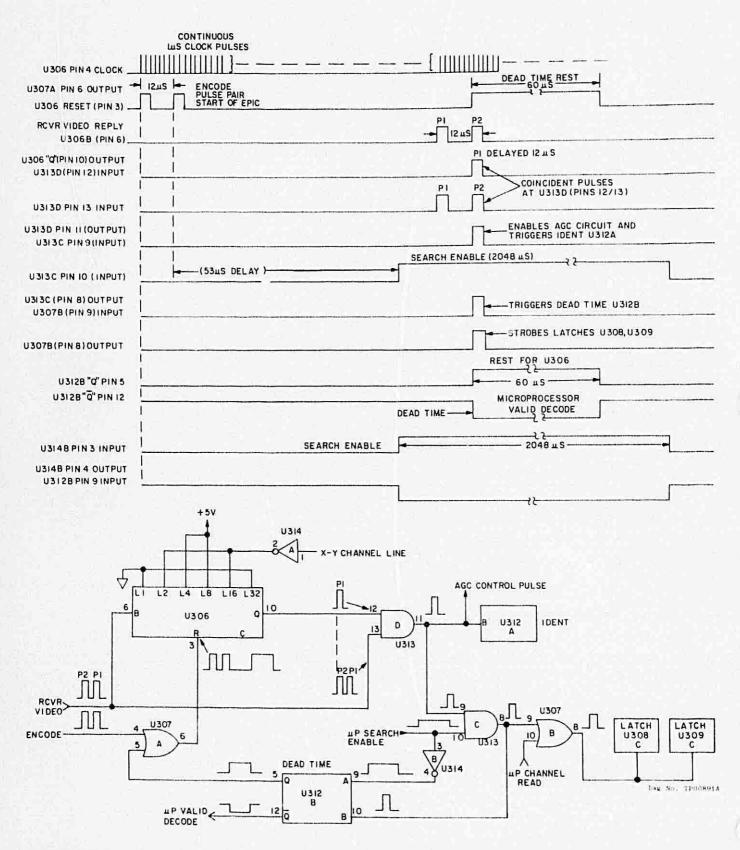


FIGURE 3-10. DECODER/DEAD TIME TIMING AND SIMPLIFIED SIGNAL FLOW SCHEMATIC

3.8.4.2 Continued

Table 3.4 shows the programming for the X-Y channels.

When the shift register (U306 is programmed for an X channel the register is clocked at a 1 us rate and 12 clock pulses thus provides a delay of 12 us. Y channel is represented by 30 clock pulses equaling a 30 us delay.

For example: Select zero KHz (X channel). The X-Y channel control select gate input (U314A, pin 1) will be logic 1.

This is inverted by U314A (to logic 0) and applied to U306 control input's L2 and L16, (See Figure 3-10) providing a 12 us delay at its Q output, pin 10.

At the beginning of a Search Track Epic, the Encode port (pin 3) of the microprocessor U319 sends 2 pulses to the reset (R) input of U306 and Q output (pin 10) will be set to logic 0. When a reply is received, the first receiver Video pulse (P1) is differentiated by C314 and R342 and applied to U306, pin 6. Diode CR319 clamps the negative differentiated spike to ground which protects the CMOS U306. The 1 us clock pulses begin to shift (delay) the data (P1). After 12 us, P1 appears at the Q output of U306 and is applied to pin 12 of U313D (Coincident AND Gate). At the same time, the second receiver Video pulse (P2) appears and is applied to pin 13 of U313D. Since both P1 and P2 are present at the same time, a single pulse appears at the output of U313D, pin 11. Thus, only properly spaced replies can pass through U313D.

The decoder reply from U313D is used in four ways:

(1) It is used by the IF Receiver to enable the AGC sample-and-Hold (AGC control pulse).

(2) It is used as a trigger for U312A the IDENT Generator.

(3) It is used as a trigger for U312B the Dead Time Multivibrator.

(4) It is used as a strobe for the latches, U308 and U309.

When U312B (Dead Time) is triggered, U306 will be shut down for approximately 60 us as the Q, output from U312B, pin 5 is applied to the reset (R) of U306.

3.8.4.3 Dead Time Multivibrator (U312B) (Figure 6-3 and Figure 3-10)

The Dead Time Multivibrator, U312B, serves to reduce the possibility of synchronizing the DME to a reflection path (Echoes). The chances of this happening at shorter ranges is much greater than at longer ranges, hence, the Dead Time of 60 us corresponds to a range of approximately 5 nautical miles.

U312B is a retriggerable, resettable multivibrator. Table 3.5 shows the A-B excitation and the response to those inputs.

At the start of a Search-Track Epic, the Search Enable line is logic low and prevents U312B from being triggered. 53 us later the Search Enable line goes logic high for the duration of the 0-160 mile count, and is inverted by U314B. U312B is now primed and ready to be triggered. Upon receipt of a valid decoded pulse (trigger) from AND gate U313C, U312B is triggered for a dead time of 60 us. The Q output of U312B is OR'ed by U307A and shuts down the Decoder, U306. The $\overline{\rm Q}$ output of U312B is the Valid Decode input signaling the microprocessor (U319) to accept the data from the latches.

TABLE 3.5. U312 EXCITATION

IN	PUTS	U312	This symbol means an input
Α	В	RESPONSE	transition from Logic High
ユ	L	NO TRIGGER	This symbol means an input
J.	Н	TRIGGER	transition from Logic Low
H	7	NO TRIGGER	to Logic High.
L	5	TRIGGER	H=Logic High, L=Logic Low
			Dwg No. TP00882A

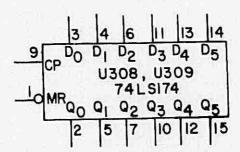
3.8.5 Search Track Counters and Latches

The microprocessor commands the Search Track Counters and Latches to operate in either of three modes: Search Track, Channel Read, and display interrupt. The microprocessor has a routine that it has been programmed to follow. This was explained in Section 3.7. Briefly that sequence is as follows: the microprocessor will initiate 15, 0-160 mile counts (a 0-160 mile count is the time taken by the counter chain to reach its terminal (end) count), and then briefly interrupt this sequence to perform various calculations, and then issue a Channel Read command.

3.8.5.1 Search Track Sequence Mode

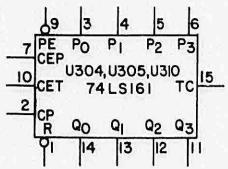
The purpose of the Search Track Mode of operation is to measure the elapsed time between the DME transmission and the ground station reply. This is accomplished by counting 1 microsecond intervals (equivalent to 0.08 mm) between airborne transmission and ground reply with a delay that cancels the Ground Stations delay.

Before proceeding with the circuit theory, a functional description of a 74LS174 latch and 74LS161 counter will be given so that their operation may be fully understood.



The 74LS174 is a high speed Hex D Flip-Flop. The information on D inputs (DO to D5) is transferred to storage (QO to Q5) during the LOW to HIGH clock transition (CP). The device has a Master Reset (MR). A logic LOW to the MR input will force all Q outputs to logic LOW, independent of clock or data inputs. (Refer to Figure 6-3, and Table 3.6)

3.8.5.1 Continued



The 74LS161 is a 4 bit synchronous binary counter that counts up to 16 in a binary sequence. It features a synchronous Parallel Enable (load). All changes of the Q outputs occur as a result of, and synchronous with, the LOW to HIGH transition of a Clock input (CP).

Three control inputs, Paralled Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET) select the mode of operation. The Count Mode is enabled when the CEP, CET and PE inputs are logic HIGH. When the PE is logic LOW, the the counters will synchronously LOAD the data from the parallel inputs (PO, P1, P2, P3) into the counter on the LOW to HIGH transition of the clock. Either the CEP or CET can be used to inhibit (HOLD) the count sequence. With the PE held logic HIGH, a logic LOW on either the CEP or CET inputs will cause the existing output states (Q0, Q1, Q2, Q3) to be retained.

The Terminal Count (TC) output is logic HIGH when the CET input is HIGH and the counter is in the 15th count of its sequence. On the 16th count, the TC returns to LOW.

The Reset (R) input, when logic LOW, overrides all other input conditions and sets the Q outputs to logic LOW.

3.8.5.1 Continued

53 microseconds after the Encode port of U319, pin 3 has initiated a DME transmission, the Search Enable port (U319, pin 5) goes logic HIGH and enables the Search Track chain. Concurrent with the Search Enable line, the data clear line goes logic HIGH releasing the counters and latches from their reset state. The Channel Read line, which is normally LOW is inverted by U314E and sets the counters to the Count Mode.

U301 feeds 1 us clock pulses continuously to the counters (U304, U305, U310) which run uninterrupted to the final count of 2048.

TABLE 5.0. DINALI COD	TABLE	3.6.	BINARY	CODE
-----------------------	-------	------	--------	------

	OU	TPUT	CLOCK PULSE		
TC	Q3	Q2	Q1	Q0	NUMBER
0	0	0	0	0	Start
0	0	0	0	1	3 1 1 -
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
1	1	1	1	1	15
0	0	0	0	0	16

Dwg. No. TP00881

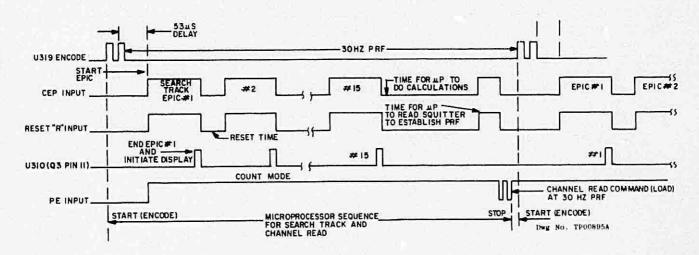


FIGURE 3-11. U304, U305, U310 CONTROL INPUTS

3.8.5.1 Continued

U305 and U310 are initially inhibited since their CET inputs are connected to the TC output of the preceeding counter and are in a logic LOW state. (Refer to Figures 3-11, 3-12, 3-13) U304 begins counting and at the 15th clock pulse its TC output goes logic HIGH. This releases U305 from its HOLD state and upon receipt of the 16th clock pulse, QO of U305 goes to logic HIGH, and the TC output of U304 goes back to logic LOW and puts U305 back in the HOLD state. U304 again goes through its count sequence which results in the Q1 output of U305 changing to logic HIGH. It has taken 32 clock pulses for U305 to reach the count of 2. In order for U305 to reach the count of 15 and release U310 from its HOLD state, it will take 255 clock pulses. During one 0-160 mile count, there will be 128 TC output pulses from U304 and 8 TC output pulses from U305. output from U310 is connected to the External Interrupt (EXT INT) port, pin 38, of U319. A logic HIGH signals the microprocessor to end the 0-160 mile count, start another and initiate the display. Since Q3 of U310 will go logic HIGH on its count of 8, it will take a total of 2048 (256 X 8) clock pulses to end the count. The microprocessor will use the EXT INT pulse as a display initiate and as a clock to limit the number of 0-160 mile counts to 15, at which time it briefly enters into a different routine. The Data Clear (counters reset) time between each of the 15 counts is approximately 90 us.

A reply pulse pair that is received during a Search Track epic and is recognized by the decoder, will strobe latches, U308 and U309, and U312B the Dead Time Multivibrator. The outputs from the counters, at the time of the latch strobe from U307B, will be transferred to the latch outputs for the microprocessor to read. The latch strobe does not stop the counters, it only samples their outputs.

During a later routine in its program, the microprocessor will review all this stored data in its memory banks and make comparisions to sort out the valid synchronous replies from the noise and ground station squitter. This data will be smoothed and used by the microprocessor to compute distance, velocity and time-to-station information. If for any reason, valid replys are not received for 10 seconds or longer, the microprocessor will signal a fault by causing "bars" to be displayed in place of the distance readout.

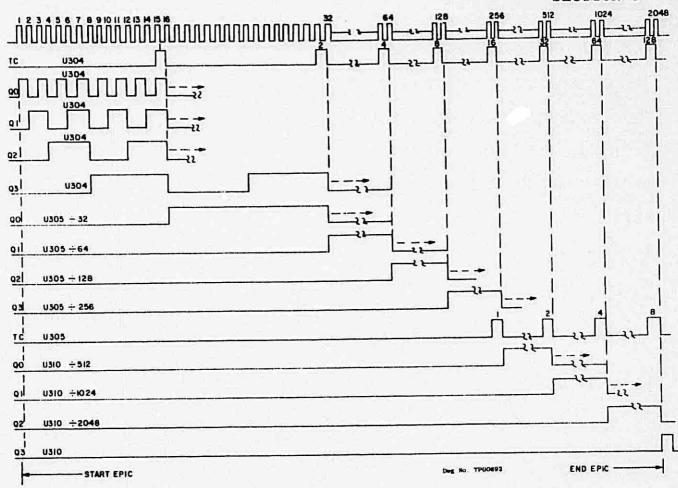


FIGURE 3-12. SEARCH TRACK COUNTERS TIMING FOR 1 EPIC

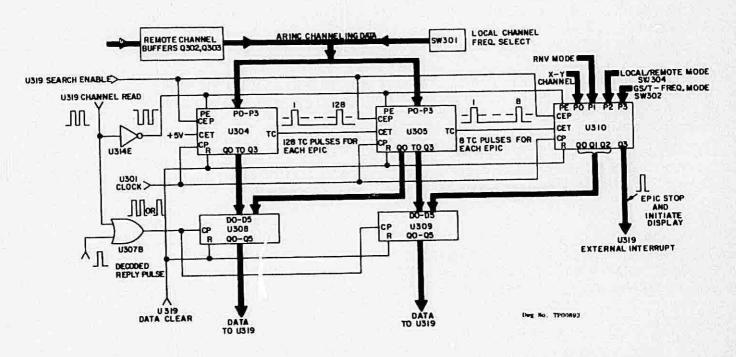


FIGURE 3-13. SEARCH TRACK/CHANNEL READ DATA FLOW

3.8.5.2 Channel Read Sequence Mode (Refer to Figures 6-3, 3-11, 3-13)

The purpose of the Channel Read Sequence is to sample the frequency control lines at a 30 Hz rate and latch this information for the microprocessor to read. At this point serial data can be sent to the digital control section of the synthesizer, in the event frequency has been changed.

In addition the following are also sampled at a (30 PRF): The RNV mode line, X-Y channel line, local-remote channel line, and the GS/T mode line.

As shown in Figure 3-11, the last routine in the microprocessor's cycle is to issue a Channel Read command. This consists of a pair or positive pulses from the Channel Read port, pin 16, of U319 which initiates the following action:

a) The Channel Read pulses are inverted by U314E and fed to the Parallel Enable (PE) inputs of the Search Track Counters. A logic LOW into the PE sets the counters into a LOAD condition and upon the receipt of the next 1 us clock pulse, the data present at the parallel inputs (PO-P3) is transferred to the outputs (QO-Q3).

b) The channel read pulses are OR'ed by U307B and strobes the latches U308, U309, which transfers the data present at D0 to D5 to the latch outputs where it is read by the microprocessor.

When a frequency is first selected, the microprocessor will issue only <u>one</u> set of data to the synthesizer digital logic control. Thereafter, as it samples the frequency control lines, it will compare new data to the old, and if the same, will take no action. However, when a new frequency is selected, the new data will not compare with the old so the microprocessor will again issue only one set of new data to the synthesizer logic.

The DME 890 uses 4 lines of the ARINC 2/5 code for frequency selection. Local or Remote Mode of frequency selection is made via the PULL RMT switch (SW304) on the front panel. Pushed in, the DME's frequencies are selected by its MHz and KHz frequency knobs. Pulled out, the DME's frequencies are selected at a remote (separate) NAV receiver.

3.8.5.2.1 Local Channeling (Refer to Figure 6-3)

The Local Channeling circuitry consists of SW304 (Local/Remote-PULL RMT) and SW301 (Frequency/Select), isolation diodes CR310 to CR318, and pull-up resistors R320 to R328. Figure 6-3 shows SW301 in the 108.00 position and Local/Remote switch, SW304, in the local position. The complete ARINC Code for the MHz and KHz section of SW301 are printed on the schematic in tabular form and show which 2-out-of-5 lines will have continuity to ground. The third section of SW301 is the X-Y channel select.

The example that follows relates the events of a channel 108.00 setting:

SW301's pin 10 (MHz), pin 13 (KHz), and pin 12 (X-Y) are connected and identified as the Co line in Figure 6-3. The contact of each pin is always making contact with its respective rotating tab. Line Co is connected to ground through the LOCAL contact of SW304.

Figure 6-3's MHz tabulation shows that, in addition to line Co being grounded, the A and D lines are grounded. The schematic pictorially shows the mating of the contact and rotating tab connected to ground (pins 3, 9, and 10).

A ground at pins 3 and 9 will pull the junctions of CR314/R325 and CR317/R328 to a logic LOW. These signals enter counter U305 at pins 6 and 3 respectively.

Figure 6-3's KHz tabulation identifies that the Co line and the B line are grounded while the Y line (channel) is open (logic HIGH). Pictorially pin 3's contact is mating the rotating tab and thus grounded via the Co line (pin 13). This pulls the junction of CR312/R322 (KHz B, pin 3) to logic LOW.

SW301's X-Y section pin 8 shown pictorially NOT making contact with the rotating tab and the junction of CR318/R324 is pulled-up to +5 volts (logic HIGH).

The X-Y channel line, is connected to counter U310, and also connected to inverter U314A that programs decoder U306 for an X channel delay of 12 microseconds or a Y channel delay of 30 microseconds. Counters U304 and U305 are used to extract the ARINC channeling data for the microprocessor while counter U310 is used to sense four special operating conditions:

1. Input PO of U310 senses the logic state of the X-Y channel line. A logic HIGH (X channel) signals the microprocessor to Encode a pulse pair of 12 microsecond spacing while the logic LOW (Y channel) will Encode a pulse pair of 36 microsecond spacing.

3.8.5.2.1 Continued

2. Input P1 of U310 senses the logic state of the RNV Mode control line. A logic LOW signals the microprocessor to activate the RNAV data lines. The input to P1 is also routed to NAND gate U311D and is used to illuminate the letters RNV in the display.

3. Input P2 of U310 senses the position of the Local/Remote (RMT) Mode switch (SW304). The junction of R329/R331 determines the logic state of the sensing line as it is connected to P2. With SW304 in the LOCAL position, P2 is pulled to logic HIGH (5 volts) through pull-up resistor R331. When SW304 is in the Remote position, R329 is grounded pulling the junction of R329/R321 LOW, thus providing a logic LOW to P2 of U310. This logic LOW signals the microprocessor to light the letters "RMT" in the display.

4. The P3 input to U310 senses the position of the GS/T FREQ. Mode switch (SW302). When the switch is in the GS/T position, P3 is grounded through R332 and gives a logic LOW input. This signals the microprocessor to display distance, velocity, and time-to-station information and illuminates the letters NM, KT, and MIN. When the switch is in the FREQ position, P3 input is connected to +5 volts (logic HIGH). This signals the microprocessor to display distance and frequency information and illuminate the letters NM and MHz.

3.8.5.2.2 Remote Channeling (Refer to Figure 6-3)

The DME 890 is capable of being remotely channeled by those NAV receivers that use the ARINC 2/5 code in their remote channeling switches.

The remote channeling circuitry consists of isolation diodes CR301 to CR309, pull-up resistors R310 to R318, isolation resistors R301 to R309, remote channeling buffers U302 and U303, and the Local/Remote Mode switch (SW304).

When SW304 is in the LOCAL position, the outputs of buffers U302 and U303 are in a high impedance state, as a logic HIGH of 5 volts through resistors R330 and R331 turns them off. This isolates the Remote Mode from the Local Mode. When SW304 is placed in the Remote position, the junction of R329/R331 goes logic LOW activating the buffers and connecting the remote channeling lines to counters U304 and U305. With SW304 in the Remote position, the common Co line from SW301 (front panel frequency select) is removed from ground, rendering the Local Mode inoperative.

3.8.5.2.2 Continued

When SW304 is in the Remote position and there are no connections to the remote channeling lines, then they will all be pulled up to logic HIGH (5 volts). The microprocessor has been programmed to sense this unique condition and will signal a fault by causing the display to flash, at a 3 Hz rate, the word "Error". When a remote receiver is connected and being used to channel the DME an incorrect ARINC code will cause the Display to read, "Error".

3.8.6 Ident Generator

The Ident generator (U312A, pin 2) is toggled by the signal obtained from the decoder AND gate, U313D. This can be noise, squitter, or Ident. The Ident signal is a Morse code identification of the ground station at 1350 Hz, actually, a regular PRF of 2700 Hz (1350 double pulses). When not transmitting Ident, the ground station transmits squitter, a random output of approximately 2700 pulse pairs per sec.

The Ident generator, R812A, is a retriggerable multivibrator (see Figure 6-3). When U312A is triggered at a regular rate, the output is approximately a 30-70% duty cycle 1350 Hz square wave as determined by the time constant of R349 and C317.

The trigger input from U313D is a positive decoded pulse comprising 2700 squitter pulses per second. Since these pulses are random, the Ident output sound is similar to that of noise. However, when Ident is being transmitted, the sound of the 1350 pulse pairs per second tone resembles the output of a tone generator.

The supply voltage to U312A is only +5 volts, making the output insufficient to generate enough audio power, therefore, U311B, an open collector NAND gate, is used to translate the output level up to +14 volts through pull-up resistor R333. This signal is then AC coupled through C321 to the Ident level potentiometer R354, which is part of the OFF-IDENT-PULL RMT switch located on the front panel.

3.8.7 Clock Generator

The clock generator provides timing pulses to the microprocessor, decoder, search track counters and the phase locked loop of the synthesizer. The clock generator comprises a crystal controlled 4.000 MHz oscillator driving the microprocessor and a 4 bit ripple counter as shown in Figure 3-14.

In the following description, the pulse periods are given on the basis of the interval between the leading edge of adjacent pulses.

The period is much easier to read and check from the calibrated time base of an oscilloscope. Refer to Figure 6-3.

The crystal oscillator comprises two inverters within U314. The first section, U314F utilizes R350 to set the operating range in its linear region. The second stage, U314D, serves as an inverter, whose outut, through capacitor C319 and crystal Y301 provides the positive feedback necessary to sustain oscillation at the crystal frequency. The clock drives the microprocessor U319, and counter U301.

U301 is a 74LS93 4 bit ripple counter. The master resets (pins 2 and 3) are grounded permanently, enabling the counter. The 4 MHz clock pulses are applied to input CPO. Simultaneous divisions of 2, 4, 8 and 16 are performed at QO, Q1, Q2, and Q3 outputs when the output of QO is externally connected to input CP1.

The divide by 4 output (Q2) provides 1 us clock pulses to the decoder U306, and Search Track counters U304, U305, and U310. The 1 us period is equivalent to 0.08 nautical mile. The divide by 16 output (Q3) provides a 4 us (250 KHz) reference clock to the phase locked loop, U403.

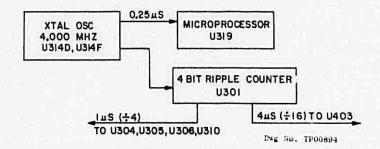


FIGURE 3-14. CLOCK GENERATOR BLOCK DIAGRAM

3.8.8 Display Assembly

For ease of discussion, Figure 3-15 is provided to identify the sections of the display.

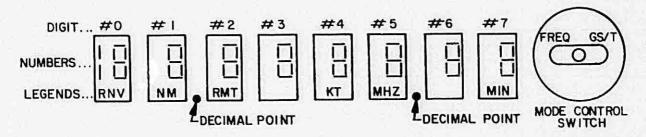
The Display Assembly consists of two parts of a gas-discharge display: one part for the numerics, identified as digit #0 through #7; the other for the legends below the numerics located in digits #0, #1, #2, #4, #5, and #7. The decimal points are located in digits 1 and 5.

The numerics use the standard single numeral seven segment format, except for digit #0. Digit #0 has two numerals to display, the hundreds (2 segments) and the tens of miles (7 segments). When below one hundred miles the hundred numeral blanks out, below ten miles the complete digit #0 is blank. Digits #3 and #6 will blank out when their reading is less than zero

The decimal point located between digits #1 and #2 provide distance resolution of 0.1 NM, while the point between digits #5 and #6 provides the frequency resolution of .05 MHz and lights only in the FREQ mode.

The Display readout is subject to the mode control switch's setting: FREQ - distance (NM) and frequency (MHz) or GS/T - distance (NM), Velocity (KT), and time-to-station (MIN).

A "bar" readout in the Display, indicating a no signal condition, will be seen by the illumination of the "g" segment of digits #0, #1. and #2.



Dwg No. TP00899

FIGURE 3-15. DISPLAY

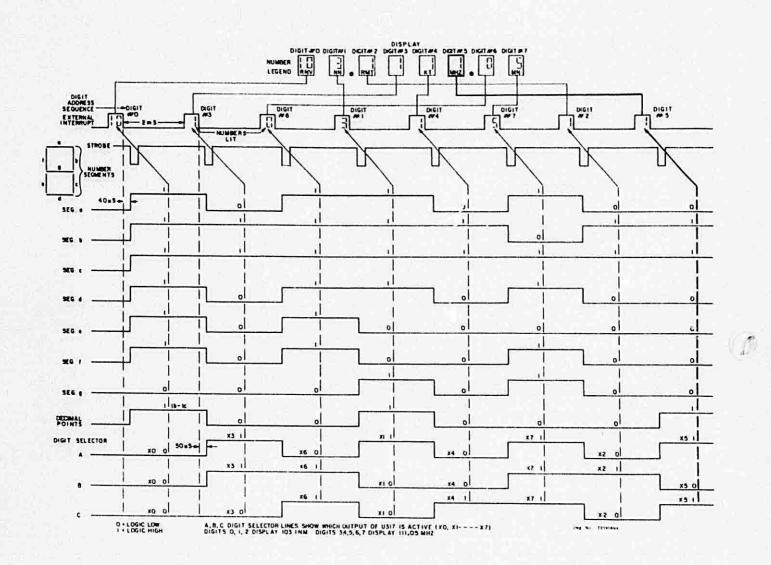


FIGURE 3-16. DISPLAY TIMING DIAGRAM FOR 103.1 NM AND 111.05 MHz, MODE SWITCH IN FREQ POSITION

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((0)

3.8.8 Continued

Refer to Figure 6-3, 3-15, 3-16, 3-17, and 3-18 for the following circuit discussion.

When the microprocessor (uP) receives an external interrupt pulse from Q3 of U310, it iniates a display by encoding the A, B, C digit select lines, the segment lines, and the strobe line. All the digits and legends are not lit simultaneously, they are multiplexed. They are not multiplexed in a straight sequence (i.e. 0-1-2-3) as this might lead to a ripple effect that could be detected by the human eye. The microprocessor has been programmed to address the digits and legends in the following sequence: 0, 3, 6, 1, 4, 7, 2, 5.

Since there are eight digits (#0 thru #7) and the external interrupt pulse occurs approximately every 2 milliseconds, it takes 16 milliseconds to complete the lighting sequence. Thus, each <u>digit</u> is selected once every 16 milliseconds for an address frequency of 1/.016 sec = 62 Hz. As each digit is selected, +100 Vdc is applied to its anode. Whatever segments are required for this digit's number must have -100 Vdc applied to their cathodes. Thus with the anode at +100 Vdc and the cathode at -100 Vdc the gas is ionized, illuminating the segment. (The intensity of the display is automatically controlled by the photocell R378, located on the front panel).

As an example of how a <u>number</u> is illuminated, a frequency of 111.05 MHa was selected and from that frequency, the <u>number</u> chosen is the last "1" of 111.05. This number (1) will be seen in digit #5's position. Follow the explanation closely with reference to Table 3.7 and Figures 3-16 and 3-17.

Forty microseconds after the receipt of the external interrupt pulse, U319 will activate segments lines "b" and "c" (Logic 1) as the numeral 1 is to be displayed in digit 5. These segment lines turn on U320, a high voltage segment driver. The outputs of U320 are connected to the emitters of Q312 and Q316 and are pulled down to approximately -100 Vdc. The collectors of Q312 and Q316 are connected to the cathodes of segments "c" and "b". When the emitters go to -100 Vdc, base current drive from Q303 in the dimmer circuit turns on Q312 and Q316 connecting the segment cathodes to current limiting resistors R368/R372. These are referenced to -100 volts at pins 13 and 16 of U320.

In order to light digit 5, an anode voltage of ± 100 Vdc must be applied while the cathode is at a potential of ± 100 Vdc.

3.8.8 Continued

Approximately 10 microseconds after the segment lines are activated, the A, B, C digit select lines are encoded. These 3 digit select lines are used to program U317, an 8 channel multiplexer, so as to address the digits in the sequence of 0, 3, 6, 1, 4, 7, 2, 5. Table 3.7 gives the programming for U317.

TABLE 3.7. U317 PROGRAM

CONT	ROL	INPU	TS	SWITCHES	DIGIT
INH.	С	В	A	ON	SEQUENCE
0	0	0	0	ХO	0
0	0	1	1	Х3	3
0	1	1	0	Xe	в
0	0	0	1	X1	1
0	1	0	0	X4	4
0	1	1	1	X7	7
0	0	1	0	X2	2
0	1	0	1	X5	5
1	Х	х	х	NONE	

Dwg. No. TP00901

The multiplexer (U317), a CMOS 14051, effectively implements an 8 PST electronic switch. As shown below, all the poles are tied to a common point (pin 3) X and referenced to +5 volts.

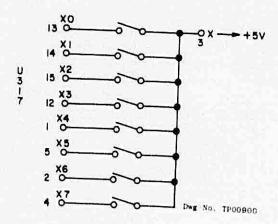


FIGURE 3-17. CMOS 14051, U317

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3.8.8 Continued

Since digit 5 is to be activated (illuminating numeral 1), switch section X5 must be closed. According to Table 3.7, this section will be turned on when digit selector line A is logic 1, B is logic 0 and C is logic 1. (Figure 3-16). When X5 is closed, 5 volts is applied to pin 5 of U315, the high voltage (+100 Vdc) digit driver. Pin 18 of U315 then applies +100 volts to the anode (pin 4) of digit The gas in segments "b" and "c" now ionize and illuminate the Included in digit #5 is the legend "MHz" that must be lit at this time. When switch X5 is closed, all other switch sections are off (logic 0). The output from switch XO is applied to noninverting buffer U303F into pin 4 of AND gate U313B and shuts this gate off. Buffer U303F is also applied to inverting gate U314C which presents a logic 1 to AND gate U313A (pin 1). Pin 2 of U313A is tied to the decimal select line of U319 (pin 27) and will also be at a logic 1 level (see Figure 3-16). Coincidence pulses at pins 1 and 2, turn on U313A and its output is applied to the passed on by The 5 volts from U307 turns on U318, a high voltage OR gate U307C. (-100V) character driver. The outputs of U318 apply -100 volts to the emitters of Q305, Q306, and Q307. Base drive from Q303 in the dimmer circuit, turns on Q305, Q306, and Q307 connecting the character's cathodes to a -100 Vdc potential through current limiting resistors R360, R361, and R364. The characters MHz are now illuminated.

As shown in Figure 3-16, the maximum time that a digit could be illuminated would be 2 milliseconds, the time between external interrupt pulses. Figure 3-16 shows the segment and digit select data lines changing their status every 2 milliseconds. Each of the 8 digits are selected to be active for 2-out-of-16 milliseconds which is approximately a 12% duty cycle. However, the actual time the digit may be illuminated during its 2 millisecond period is modified by the dimmer circuit.

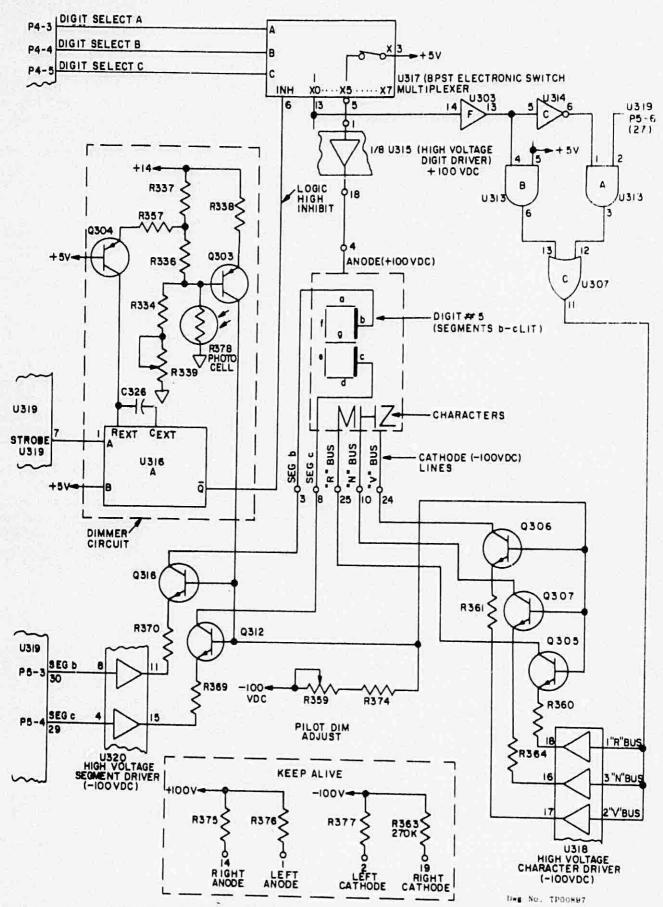


FIGURE 3-18. SIMPLIFIED DISPLAY DIAGRAM

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3.8.8.1 Dimmer

The Dimmer circuit is comprised of U316A, (a one shot multivibrator), photocell R378, transistors Q303, Q304 and associated resistors. Refer to Figure 3-18. The dimmer circuit has a twofold duty to perform: it must control the base drive to the segment and character transistors (Q305 to Q316) which affects the intensity of the digits by controlling the current, and it must enable the multiplexer U317 which also affects the intensity by controlling the duty cycle.

During the 2 millisecond period a digit is active, the segment and character cathodes have a continuously applied negative potential on them. However, the $\overline{\mathbf{Q}}$ output of U316A will inhibit the multiplexer (U317) for a portion of the 2 millisecond period depending on the brightness. Table 3.7 shows that when U317 receives a logic 1 to the logic high inhibit (INH) input, all the switch sections are turned off. This removes the anode voltage from the digit and shuts it off. The Dimmer circuit operation will be described using Figures 3-16 and 3-17 as guides.

The photocell (R378), located on the front panel, is used to establish the base voltage at Q303 and the potential at the junction of R336/R337. The photocell can encounter two extreme boundries: namely, brilliant sunshine and low intensity light from the instrument panel during night flying. Under brilliant light conditions, the digits must be at their highest intensity which means the multi, U316A, will have a long "on" time. Dark conditions require a short "on" time. The ohmic value of photocell R378 can change from several megohms under dark conditions to less than 1K ohms under brilliant sunlight. If the light in the cabin is very bright then R378 will clamp the base voltage at Q303 to approximately 7 volts. This turns on Q303 relatively hard, which increases the base drive to the segment and character transistors. This will result in a greater current flow through the segments and characters which will raise their intensity.

3.8.8.1 Continued

Resistor R357 and transistor Q304 in conjunction with capacitor C326 form the external RC timing circuit which determines the "on" time of U316A. The voltage potential at the junction of R336/R337, (controlled by R378), determines how fast C326 (timing capacitor) charges up. A low voltage at R336/R337 results in a longer charge time which increases the "on" time to U316A. A higher voltage results in a shorter "on" time.

As shown in Figure 3-16, less than 1 microsecond after the digit selector lines are activated, the microprocessor issues a strobe pulse (pin 7, U319) to U316A (pin 1). This triggers the multivibrator and its \bar{Q} output (that was logic HIGH prior to the trigger) releases U317 from its inhibit state. Under very bright light, the "on" time of U316A may be very close to the total 2 millisecond period the digit is active. Under dark conditions, the "on" time may be as low as 200 microseconds. Thus the digit's intensity is controlled by regulating the current and actual "on" time. Resistor R359, is adjusted at the factory to set the upper limit of intensity.

Resistor R339 is accessible through the front panel and the display intensity can be adjusted according to the pilot's preference at the dark end only. This adjustment is minimal.

The Display Assembly has a Keep Alive feature that provides the digits with a voltage to keep the gas in a constant state of low level ionization. This feature assures instantanious illumination, especially in a cold environment.

The Keep Alive circuit consists of two sections: Left and Right as shown in Figure 3-17. Resistors R375/R376 connect to the +100 Vdc to the anodes, and resistors R377/R363 connect the -100 Vdc to the cathodes.

3.8.9 Frequency Synthesizer Description

The frequency synthesizer drives the Exciter section of the transmitter and provides a local oscillator (LO) signal to the superheterodyne receiver. The synthesizer, operates from 520.5 to 575.00 MHz, that is 1/2 of the transmitters frequency range of 1041 through 1150 MHz.

The basic frequency of the ÷N digital synthesizer is controlled by the 4 microsecond (0.25 MHz) reference pulses from U301, the output frequency, however, is selected via frequency channel select knobs.

The calibrations of the channel selector are 108.00 through 117.95 MHz, the VHF frequencies of the paired VOR/DME channels. The actual paired DME transmit frequencies are 1041 through 1150 MHz. Table 3.1 provides paired frequency versus VCO frequency information. When the pilot sets his frequency controls, the synthesizer logic produces a VCO control voltage that sets the VCO to the required operating frequency for that channel. The control voltage applied to voltage variable capacitor CR401 determines what its effective capacitance will be. This capacitor and C404 are series connected across L401 to form a tank circuit that determines the frequency of the VCO.

The following describes synthesizer operation when channel 116.9 MHz (see Table 3-8: 116 X = VOR 116.9-- transmitter 1140 MHz, synthesizer 570 MHz) is selected by the front panel MHz and KHz knobs. Refer to Figure 6-3 schematic and Figures 3-19 and 3-20.

TABLE 3.8. ARINC TO SYNTHESIZER CODE CONVERSION

		put W30	fr	om	Ou	tput U32		m			put W30		om	Output from U321				
MHz	A	В	C	D	A8	A4	A2	A1	KHz	A	В	С	D	B8	B4	B2	B1	
108	0	Х	Х	0	Х	0	0	Х	.0	X	0	X	Х	X	0	0	X	
109	0	x	х	х	Х	0	0	0	,1	0	0	X	X	Х	0	0	0	
110	х	0	Х	Х	0	х	х	Х	. 2	0	Х	0	X	0	X	X	X	
111	0	0	х	x	0	X	х	0	. 3	X	o	0	X	0	X	X	0	
112(,0/,2)	0	X	0	Х	0	х	0	Х	. 4	Х	0	X	0	0	X	0	X	
112(,3/.9)	0	х	0	х	0	Х	0	0	. 5	X	x	0	0	0	X	0	0	
113	x	0	0	Х	0	0	X	X	.6	X	X	0	X	0	0	X	X	
114	x	0	x	0	0	0	X	0	.7	X	X	X	0	0	0	X	0	
115	x	x	0	0	0	0	0	х	.8	0	X	X	0	0	0	0	X	
116	x	х	0	х	0	0	0	0	.9	0	X	X	X	0	0	0	0	
117	х	x	х	0	х	X	X	X	les o			7.						

X= LOGIC HIGH O= LOGIC LOW

Dwg. No. TP00910

The VCO is locked at 570 MHz, 1/2 the transmitted frequency, by the VCO control voltage obtained from the logic. The 570 MHz frequency is connected through buffer Q402 to RF amplifier Q403, into a ÷2 prescaler. The prescaler is a push-pull oscillator comprised of Q404, Q405 and L406. With the 570 MHz input the prescaler output is 285 MHz and is fed to the ÷N counter chain. For the example chosen, "N" is equal to 1140.

The panel's MHz/KHz selection switches are not in binary form, they are in the ARINC 2/5 code form. Additionally, there is a transmitter output frequency of 11 MHz jump between 112.2 and 112.3 MHz. A code conversion is required to change these switch outputs to the required Binary format. The microprocessor is programmed to provide this code conversion. Table 3.8 shows the input to output code.

Continuing the example, 116.9 MHz was chosen. When this frequency is set, the microprocessor will send a channel clock and serial data to U321, a serial in/parallel out shift register. This data and clock is sent only one time per frequency selection. Note in Table 3.8 that the MHz code lines (A8, A4, A2, A1) from U321 are all logic LOW as are the KHz code lines (B8, B4, B2, B1). These data lines are connected to the inputs of U405, U407, and U408, that are 4 bit high speed binary counters that count by 16. Refer to Figure 6-3.

The 285 MHz from the $\div 2$ prescaler is capacitive coupled into U401, an ECL 11C90 650 MHz $\div 10/11$ prescaler. The Mode Control (M2 pin 3) input contr-1s the count sequence. A logic HIGH to M2 sets U401 in the $\div 10$ mode while a logic LOW sets it to a $\div 11$ sequence. The output from U401, (QTT pin 11) serves as a clock for the 4 bit counters, U405, U407 and U408.

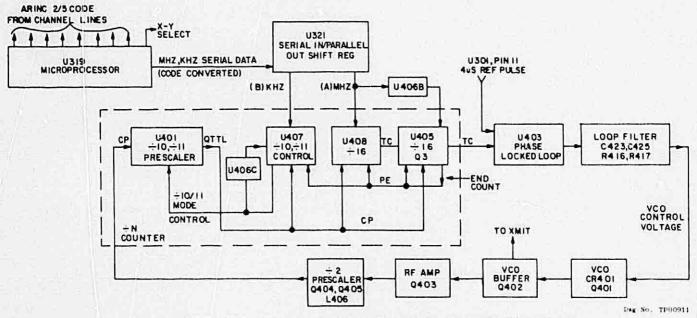


FIGURE 3-19. SYNTHESIZER BLOCK DIAGRAM

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When the ÷N counter has reached its end count, Q3 (pin 11) of U405 goes logic LOW. Q3 is connected to the parallel enable (PE) inputs of U405, U407, U408. When the PE input is logic HIGH the counters are set in the Count Mode, when PE is logic LOW, the counters are set in the Load Sequence. In our example, the ÷N number is 1140 and the count sequence will begin after the counters are loaded. Refer to Figure 3-19 and 3-20.

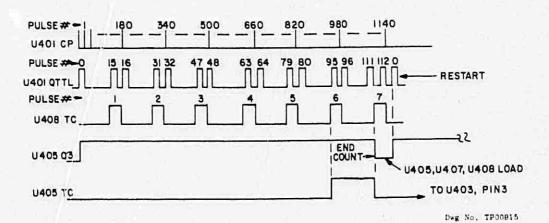


FIGURE 3-20. SYNTHESIZER DIGITAL TIMING FOR 116.90 MHz

When Q3 of U405 goes logic LOW, upon a receipt of the next clock pulse from U401, the data at the inputs to the counters are transferred to the outputs. KHz lines B8 to B1 and MHz lines A8 to A1 are logic LOW. MHz lines A8 to A4 are connected to NAND gate U406B which inverts the inputs and gives a logic HIGH to P0 (pin 3) of U405. Note that P1 and P2 are tied to ground and P3 is tied to +5 volts. This presets into the inputs of U405 the number 9 (1001). Therefore this counter only needs to count from 9 to 16 to finish its count.

When the inputs are transferred to the outputs, Q3 of U405 goes logic HIGH and sets the counters in the Count Mode. Q3 and Q1 of U407 go logic LOW. This is inverted by NAND gate U406C and sets the Count Enable Parallel (CEP) to logic HIGH which enables the U407 counter. The logic LOW at Q3 and Q1 will pull the junction of R420, R421, and R422 to logic LOW which sets U401 (M2 pin 3) in the ÷11 count mode. Note that the Count Enable Parallel (CEP pin 7) input to U405 is tied to the Terminal Count (TC pin 15) output of Q408. A logic HIGH to a CEP will enable the counter while a logic LOW input will put the counter in the "HOLD" mode, freezing the outputs at the state prior to the HOLD command. A TC output is a fully decoded output and will go logic HIGH on the count of 15 and return to logic LOW on the 16th count. Since U405 only needs to count from 9 (preset) to 16, it will require 7 TC pulses from U408 that will enable U405 to count for the period that the TC output is logic HIGH.

As the count begins, the 285 MHz pulses into U401 are being divided by 11. The Q3 (÷16) and Q1 (÷4) outputs are connected to NAND gate U406C and as shown in Figure 3-19 when both are logic HIGH, the output of U406C goes logic LOW, freezing (HOLD) the counter U407. The logic HIGH at Q1 and Q3 allows the junction of R420/R421/R422 to rise to +5 volts which now sets U401 in the ÷10 mode. U401 is now locked in the ÷10 mode for the rest of the count. At this point in time note that 120 of the 285 MHz pulses have been counted and U401 has put out 11 clock pulses. On the 15th clock pulse from U401, the TC (pin 15) output of U408 goes HIGH and on the 16th clock pulse goes LOW.

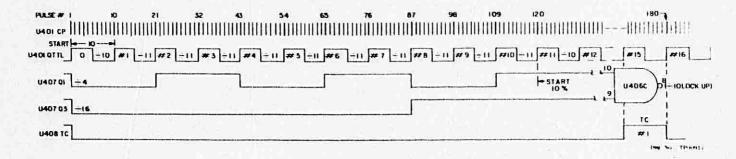


FIGURE 3-21. ÷10/11 MODE CONTROL SEQUENCE

This is the first of 7 TC pulses needed by U405 to complete its count. At this point in time, 180 of the 258 MHz pulses have been counted. Since U401 is now dividing by 10, it will take 160 of the 185 MHz pulses to give a TC output. Since 6 TC pulses are still needed, then 960 (160 X 6) of the 285 MHz pulses are required to complete the count. The total number of pulses counted will be 1140 (180, first TC, + 960, 6TC). On the 1140th pulse, Q3 of U405 goes LOW, commanding the counters to LOAD and count sequence will begin again.

The decoded TC output from U405 is applied to the Phase Comparator B (PCB pin 3) input of the phase locked loop, U403. In addition, a 4 microsecond (.25 MHz) reference is applied to the Phase Comparator A (PCA) input. If any difference in frequency exists (out-or-lock mode), the comparison of this 4 us clock against the divided down VCO frequency produces an error signal from the Phase Comparator 2 (PC2 pin 13) output. The error signal is filtered by C423, R416, R417, and C425 and applied to Varicap CR401 that controls the frequency of the VCO. This closed loop causes the output (TC) of U405 (in-lock-mode) to be a 4 us repetitious waveform into the PCB input of U403.

Referring to Figure 6-3, the VCO has two output paths. The first path is through L401, L402 and buffer Q402. The direct high-level output of the buffer, through impedance matching inductor L403, serves as an excitation of approximately +2 dBm into the exciter section of the transmitter. The purpose of inductor L404 is to parallel resonate with the parasitic capacity of Q402 that raises the impedance at the collector.

The second path is from the buffer Q402 into the RF Amplifier Q403. The gain of the amplifier is approximately 20 dBm. L405 is used to parallel resonate the parasitic capacity of Q403. The output of Q403 is coupled into the ÷2 oscillator through capacitor C414 and serves to lock the oscillator to 1/2 the VCO frequency.

Q404 and Q405 act as a push-pull oscillator that will run free at some frequency near the center of the band (270 MHz). Circuit operation is as follows: Inductor L407 is a high impedance to the 270 MHz and a DC return path for the biasing network. Current drawn through L407 passes through diodes CR402 and CR403, resistors R412 and R413, and also through resistor R401, back to -14 volts. This establishes approximately -5.5 volts at the junction of R401 and R409 that is the common bias line for all the transistors in the VCO chain.

Inductor L406 has a parasitic capacity distributed across its windings which forms a tank circuit in the collectors of Q404 and Q405 whose resonant frequency is 270 MHz. Because of dissimilar Betas (hFe) in Q404 and Q405, one will turn on before the other. Assume that Q404 turns on first. The collector of Q404 is pulled down toward -14 volts and the parasitic capacitor across L406 begins to charge toward -14 volts. Initially, the rate of change or charging current generates an EMF in L406. When the charging current drops off to the steady state (quiescent), the stored energy in the inductor collapses and generates a counter EMF at the junction of L406 and L407. This negative voltage transition back biases CR404 and is coupled through the parasitic capacitor associated with this diode and turns off Q404. As the magnetic field in L406 is collapsing, the collector of Q404 falls back toward ground potential. When Q404 is turned off, Q405 turns on and repeats the sequence. The VCO frequency (550 MHz) is coupled into the common emitters and locks the oscillator to 1/2 the VCO frequency.

Capacitor C416 (across L407) is used to balance the oscillator coil, L406, as the other side of L406 is capacitive coupled into the $\pm 10/11$ prescaler, U401.

12/80 3-49

3.9 POWER SUPPLY

Refer to Figures 3-22 and 6-4.

The power supply section consists of: a switching regulator, a DC/DC converter, two 5V regulators, and a 8V regulator. The input voltage, 14 or 28 Vdc, is connected to the switching regulator that supplies a highly regulated, low ripple +7.5 Vdc to the DC/DC converter and two +5V regulators.

The DC/DC converter provides:

-14V to the Synthesizer VCO +14V to the Receiver, Ident, and Transmitter +60V to the Modulator +100V for Gas Discharge Display

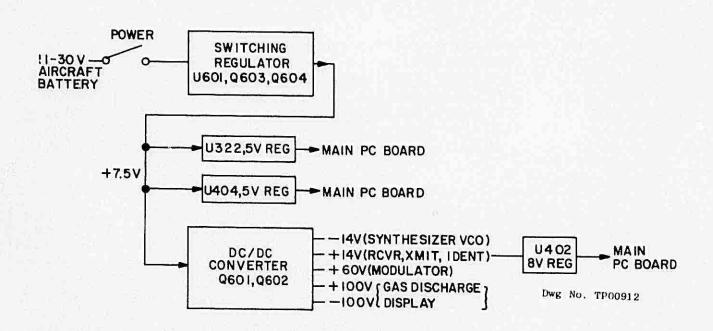


FIGURE 3-22. POWER SUPPLY BLOCK DIAGRAM

3.9.1 Switching Regulator

Refer to Figure 3-23 and Figure 6-4.

The method by which an LM205 (U601) voltage regulator is used as a switching regulator can be explained with the aid of Figure 3-22.

Basic operation is controlled by U601 (LM205). If a difference of potential is sensed when the output voltage is compared with an internal Zener diode, the output from the regulator will turn on Q603 and Q604 by means of a pulse waveform with a given duty cycle. The voltage divider, comprising R607/R608/R609, provides the voltage sensing input (pin 6) to the voltage regulator.

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3.9.1 Continued

The control pulses from the voltage, regulator (pin 2 turn on Q604, which supplies base drive to Q603 and turns on Q603.

The voltage at the emitter of Q603 will be as shown in Figure 3-23.

During the on time (t on), storage capacitor C608 will charge up to 7.5 volts. When the output voltage is correct, there is no error voltage to sense so the voltage regulator turns off Q604 and Q603. During the off time (t off), the magnetic field in the storage coil L602 will reverse its polarity. The voltage potential at the junction of L602 and CR611 now becomes negative and is clamped to ground by catch diode CR611. The field in L602 now collapses and supplies a charging current to C608 which tries to maintain a constant output voltage level. However, the current demand from the DME will cause a decrease in the output voltage level. This imbalance will be sensed by the regulator and Q603/Q604 will again turn on and charge up C608. The output of the LC filter (C608, L602) will be the average value of the switched waveform. Changes in input voltage can be compensated for by varying the duty cycle of the switched waveform.

The internal amplifier loop gain controls the ripple content of the output voltage. Feedback resistor R612 sets the differential amplifier loop gain and is selected to give maximum stability of the loop, which is maximum gain with minimum noise and ripple.

Resistor R611 establishes the base drive for Q604. Resistor R610 protects U601 under conditions of high current demand. Resistor R606 is used to help the regulator maintain a constant 7.5 volts at its output when the input voltage is at the upper limit. A high voltage at the imput is divided down by R606 and R607/R608/R609 and slightly raises the sensing input level at pin 6 of U601. When the 7.5 volt output falls below its desired level, then the increase in level at pin 6 or U601 requires less of an increase of the duty cycle from the regulator.

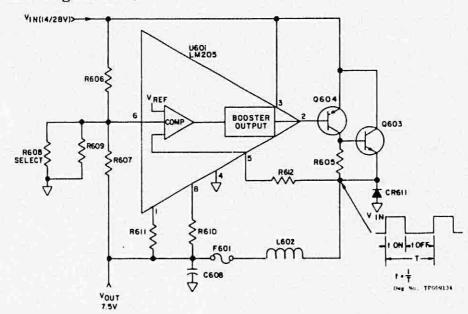


FIGURE 3-23. STEP-DOWN SWITCHING REGULATOR

3.9.2 DC/DC Converter

Refer to Figure 6-4.

The DC/DC Converter increases the +7.5 volts to +14, -14, +100, -100 and +60 volts DC. The converter is comprised of switching transistors Q601/Q602, transformer T601, and rectifier diodes CR601 through CR610. The transformer secondaries provide a voltage step-up of the 7.5 Vdc input. The rectifiers provide full wave rectification for all output voltages.

When power is first applied to PNP transistors Q601/Q602, one will turn on first because of a dissimilarity between their turn on times. For example, assume Q602 turns on first.

Q602 is initially turned on by the current from the 7.5 Vdc flowing via R603/R604 to ground, and through T601's pins 40/41 to its base. Q602 is held on for the balance of the first half cycle by the negative voltage induced in T601's windings (pins 40/41) by transformer coupling to the primary (T601 pins 13/14). An opposite polarity voltage is induced at T601 pins 47/48 during the time Q602 is on and holds Q601 off.

As long as Q602 is on and in saturation, there is a constant voltage across the primary which generates a linear rise of current. This rate of change of current with respect to time (di/dt) flowing in the primary inductance (L) generates a voltage (E = Ldi/dt) in all the secondary windings. The transformer core of T601 exhibits a square magnetic hysteresis loop and when the transformer flux density reaches saturation there can be no further generated voltages in the windings. The induced voltages in the windings now collapse and reverse their polarity. Thus the base of Q601 is now driven negative which turns it on while the base of Q602 is driven positive which turns it off. The same collapse of the base drive to Q601 occurs as the transformer core saturates in the other direction and the same flipover to turn on Q602 occurs. This process continues with the transformer moving cyclically over its entire hysteresis loop. This design is known as a push-pull square wave power converter.

3.9.2 Continued

Each of T601's ten windings are highlighted by a dot. (See Figure 6-4). The significance of the dots relate to the polarity of each winding and are for reference purposes.

Figure 3-24 shows some of the waveforms of the DC/DC converter. The square waves of voltage that drive the primary of T601 yield square waves of voltage at the secondaries. These secondaries, followed by rectifiers, generate positive and negative DC output voltages. The output beyond the rectifier diode will have a DC level of one diode drop below the peak secondary voltage. Filter capacitors are placed at the output of each pair of rectifier diodes. The operating frequency of this circuit is approximately 15 KHz.

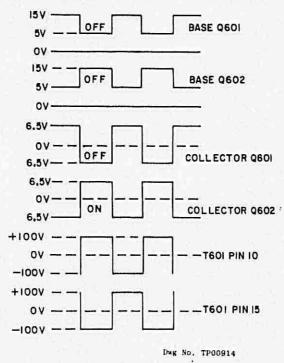


FIGURE 3-24. DC/DC CONVERTER WAVEFORMS

NARCO AVIONICS DME 890

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4.1 THE MICROPROCESSOR CONTROLLED DME 890

Semiconductor manufacturers have given the avionics designers a powerful new tool with which to advance the "state-of-the-art" in avionics, the microprocessor. The use of a microprocessor in a design means that, the unit will weigh less, grow smaller in size, have a much higher functional density, use less power to accomplish the same tasks, and exhibit greater reliability.

The microprocessor in the DME 890 accomplishes in one chip what it took two boards full of integrated circuits in the DME 190/195 to accomplish. The use of a microprocessor that controls the DME may create a very poor type of troubleshooting practice among those avionics technicians who feel inadequately trained in the new generation of microcircuitry. This poor troubleshooting practice is called "BLAME THE MICROPROCESSOR". What this means, of course, is that if a malfunction occurs in the DME, then its got to be the microprocessor's fault. This type of oversimplification must be avoided by the avionic service technician. Narco has great confidence in the 3872 microprocessor and feels that it is the least likely component to fail.

This maintenance section provides information, in the form of troubleshooting flow charts that provide a systematic approach to remedy a malfunctioning circuit or component. In addition, alignment and adjustment procedures are given in Section 4.5.

4.1.1 The 3872 Single-Chip Microprocessor (uP)

The 3872 is a complete 8-bit microprocessor on a single MOS integrated circuit. The device features: 4032 bytes of ROM, 64 bytes of scratchpad RAM, 64 bytes of executable RAM, a programmable binary timer, 32 bits of I/O, and a single +5 volt power supply requirement.

The four complete bidirectional input/output (I/O) ports (PO, P1, P4, P5) consisting of 32 lines which are divided into groups of 8, can be individually used as either TTL compatible inputs, or as latched outputs. The standard output configuration of these lines are shown in Figure 4-1. The Reset and External Interrupt lines are an open drain type, (See Figure 4-1).

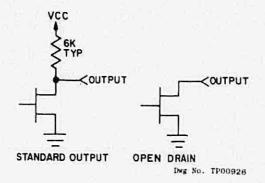


FIGURE 4-1. RESET AND EXTERNAL INTERRUPT

4.1.1 Continued

CAUTION: All the standard precautions that apply to MOS devices should be observed. Any output line shorted directly to a voltage source will destroy the output port.

WARNING: It is not recommended that a ohmmeter be used to troubleshoot this device as the meter's high battery voltage may cause damage.

<u>CAUTION</u>: If it becomes necessary to replace the microprocessor the following procedure is recommended:

1. Read Section 4.1.2.

2. Cut every pin on the microprocessor as close to the top of the chip as possible. This will leave a pin length long enough to be handled by a long nose plier.

3. While unsoldering each pin, pull the pin from the PC board with the long nose plier as soon as the solder melts.

4.1.2 A Word About Soldering Irons:

Probably every service technician, who worked on printed circuit boards, has at sometime during his career, ruined a board by using a soldering iron that was so hot that it destroyed the bond between the track and the board. Separation of the conducting path or plated through holes can be avoided by using a soldering iron controlled by Powerstats, Variacs, or soldering irons having temperature sensing tips.

Tip temperature of the iron should not exceed $600^{\circ}F$ to safely remove components from a PC board.

A few temperature controlled soldering irons (and tips) are:

Ungar Type 50T6 600°F (120 Vdc)

Ungar Type 60T6 600°F (24V)

Weller Type WTCPN w/ 600°F Temp Sensing Tip(s)

Above irons selected from Catalog 104: Newark Electronics 500 N. Pulaski Rd. Chicago, Ill 60624

(312-638-4411)

4.2 WIRING

The DME 890's construction is modular with a wiring harness interconnecting the Main PC Board to the Transmitter, Receiver, and Power Supply modules. Wires in the harness are connected to the PC boards by solder.

TABLE 4.1 PC BOARD IDENTIFIERS

Symbol Number Series	Circuit	Schematic Figure No.
100's	Transmitter	6-2
200's	Exciter	6-2
300's	Main PC Board	6-3
400's	Synthesizer (on Main PC Board)	6-3
600's	Power Supply	6-4
700's	Receiver	6-5
800's	Miscellaneous (Internal Interconnect Wiring)	6-1

4.3 MAINTENANCE

4.3.1 Basic DME Control Circuits

Before attempting to isolate any trouble in the DME, knowledge of the circuit operation is necessary, refer to Section 3 for the Circuit Descriptions. As shown in Figures 4-2, 4-3, and 4-4, some circuits provide basic clock and control signals that are necessary to the operation of other circuits. The basic conditions required for circuit operation are discussed in the following text.

4.3.1.1 RF Generation and Control

Refer to Figure 4-2. The clock generator (U314 D/F) provides timing signals for the microprocessor and synthesizer, however, +5 Vdc operating power must be obtained from two 5 volt regulators which receives its operating voltage of +7.5 Vdc from the switching regulator. The DC/DC converter requires +7.5 Vdc from the switching regulator to produce higher operating voltages. The synthesizer provides the correct frequency to the exciter section of the transmitter only when channel clock and data have been sent to the synthesizer digital section from the microprocessor. A synthesizer or microprocessor malfunction would affect both the receiver and transmitter. The transmitter provides an output when the following takes place:

- 1. An encode pulse pair from the microprocessor enables the modulator.
- 2. The modulator pulse pair (X channel = 12 us, Y channel = 36 us) are applied to the transmitter to develop the RF power.
- 3. The microprocessor sends channel clock and data to the digital section of the synthesizer.
- 4. The RF synthesizer sends 1/2 transmit frequency energy to the transmitter.

A clock generator malfunction would affect the microprocessor, receiver, and transmitter operation.

These operating characteristics may be utilized in planning an approach to troubleshoot the DME 890's transmitter or receiver. An overall check is as follows.

A check for +14 volts, -14 volts, +60 volts from the DC/DC converter confirms operation of the switching regulator (7.5 volts) and DC/DC converter.

A check for transmitter output confirms: operation of the DC/DC converter, 5 volt regulators, 8 volt regulator, microprocessor, pulse modulator, synthesizer, exciter transmitter, and frequency (ARINC) data lines.

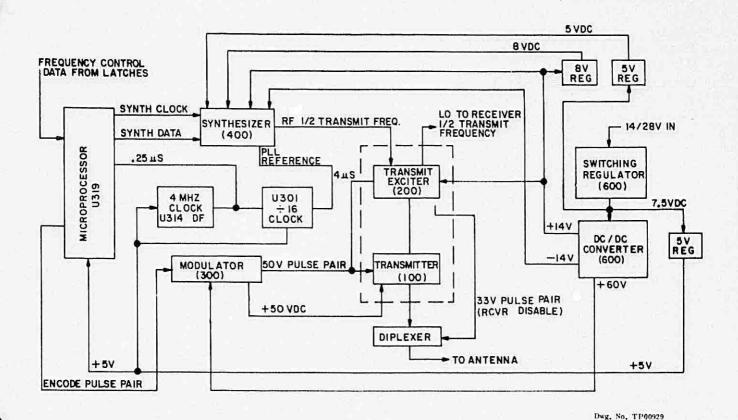


FIGURE 4-2. RF GENERATION AND CONTROL

4.3.1.2 Receiver/Search-Track Sequence

Refer to Figure 4-3. The basic receive cycle starts when a reply from a ground station has been received at the diplexer and is fed to the receiver. The receiver detects the reply and the decoder processes the video by recognizing the pulse spacing (X = 12 us, Y = 30 us). This decoded data (a single pulse) then activates the receiver AGC, triggers the IDENT, triggers the DEAD TIME (valid decode) and strobes the latches.

53 microseconds following a encode pulse pair, the search enable and data clear lines from the microprocessor are activated and the counters begin counting. Any received reply that is processed properly by the decoder, will provide a strobe to the data latches which will sample the state of the counters at this time. Also at this time the dead time multivibrator is strobed and the decoder is inhibited for approximately 60 us. A clock malfunction at U314 D/F would affect: the uP, search-track counters, and the decoder operation. A synthesizer malfunction would affect: synthesizer, receiver, and search/track operation. These operating characteristics may be utilized in planning an approach to troubleshooting the receiver or search/track operation. An overall check of the receive/search track sequence is as follows:

A check for receiver video pulses confirms operation of the receiver with its AGC circuits. A check for the data latch strobe confirms operation of the decoder and 1 us clock circuits. A check of the uP external interrupt line confirms operation of the microprocessor, counters, dead time, and clock circuits.

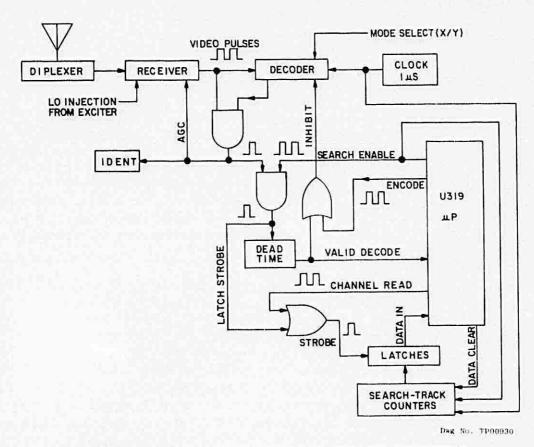


FIGURE 4-3. RECEIVE/SEARCH-TRACK SEQUENCE

4.3.1.3 Display Operating Sequence

Refer to Figure 4-4.

The basic display sequence begins when the external interrupt pulse from the search track counter is received by the microprocessor. The microprocessor will: encode first the segment lines, second the digit select lines, and then the strobe line. The microprocessor has been programmed to select the digits and characters in the following sequence: 0, 3, 6, 1, 4, 7, 2, 5 (digits are numbered 0 thru 7). When a digit is selected, +100 volts is applied to its anode and concurrently, whatever segments are required for that digit, the segment lines apply a negative volt to the cathodes. Each digit is active for approximately 2 milliseconds. Since there are 8 digits, it will take 16 milliseconds to run through a lighting sequence.

Automatic dimming is accomplished by means of a photocell located on the front panel of the DME 890. This photocell controls two functions in the dimmer circuit. The first function is a multivibrator which is being triggered approximately every 2 milliseconds by the strobe pulse from the microprocessor. The photocell determines the "ON" time of the multivibrator whose output is connected to the inhibit port of the 8 channel multiplexer. This will directly affect how long a digit will have its anode connected to +100 volts and, therefore its intensity.

The second function controlled is a transistor whose purpose is to supply base drive to the segment driver transistors. By controlling the segment drivers, the current flow through the gas-discharge display is controlled and therefore, its intensity.

A malfunction of the clock, microprocessor, search track counter, and DC/DC converter would affect the display operation. An overall check of the display is as follows:

(1) A check of the strobe pulses confirms the operation of the search track counters and microprocessor.

(2) A check at the digits character and segment drivers confirms operation of the microprocessor, DC/DC converter, 8 channel multiplexer, and dimmer circuit.

(3) A check of the photocell by blocking light from it, confirms operation of the dimmer circuit.

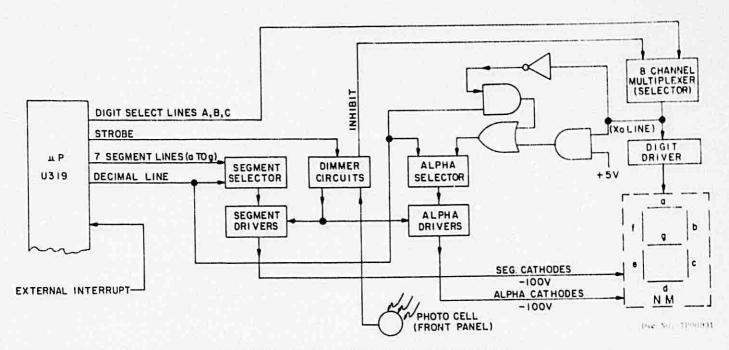


FIGURE 4-4. DISPLAY SEQUENCE

4.4 TROUBLESHOOTING FLOW CHARTS

The troubleshooting procedures are given in flow charts, Figures 4-8 thru 4-14. The first flow chart, Figure 4-8, provides a testing sequence for an operational checkout without removing the DME's dust covers. Subsequent flow charts provide a testing sequence of all the DME circuitry.

The flow of the charts leads the user down the page as each question is answered YES. A reply of NO directs the user to the right. This organization also allows quick recognition of interdependent circuits.

Troubleshooting sometimes requires leaving one circuit (Flow chart) to go to another. Thus the charts have related cross reference notations referred to as KEYs. Each key number is used twice, once on the originating drawing and at its destination drawing.

4.4.1 Functional Checkout Flow Chart (Figure 4-8)

This first level flow chart permits checkout of the DME 890 in the "Frequency" mode, or "GS/T" mode without removing the dust covers. The DME Signal Generator permits simulating operating conditions and observing the front panel display for each function. If each decision has a "YES" answer the DME operation is correct. If any decision has a "NO" response, the DME is not operating properly and the "NO" line identifies what flow chart to consult.

4.4.2 Trouble Isolation Flow Charts, Component and Circuit Level

Having confirmed that the DME is not operating properly through the use of the Functional Checkout Flow Chart, Figure 4-8, a specific flow chart is then used to locate the circuit or component at fault. These flow charts must be used in conjunction with the waveforms in Section 4.6 for signal interpretation. It is considered that a great percentage of DME faults will be evident at the points indicated in the flow charts.

4.5 ALIGNMENT AND ADJUSTMENT

Connect equipment as shown in Figure 4-5.

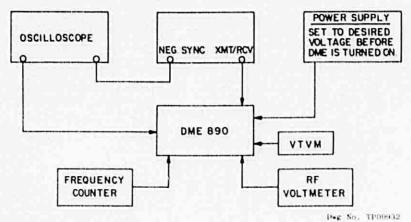


FIGURE 4-5. TYPICAL BENCH SET-UP

4.5.1 Frequency and Pulse Measurements

4.5.1.1 Clock Generator Checkout and Adjustment

- (a) Apply power to DME 890.
- (b) Connect frequency counter to crystal oscillator output U314D pin 8.
- (c) Frequency should be $4.000000 \pm 100 \text{ Hz} (+4.000100; -3.999900)$.
- (d) If frequency is not within these limits, change value of capacitor C319 to obtain correct clock frequency.

4.5.1.2 Synthesizer Checkout and Adjustment

The frequency synthesizer checkout comprises a check of the VCO frequencies and power at P401, throughout the band. See Table 3.1 for a list of the VCO frequencies. The procedure for adjusting the VCO control voltage and power output is as follows:

- (a) Connect frequency counter to VCO buffer output at P401.
- (b) Set channel switch to 117.90 MHz. The frequency counter reading shall be 575.0 MHz -50 ppm* (28.75 KHz).
- (c) Connect a DC voltmeter to VCO control line (junction of R416/R417). Voltage should be 7.2 -0.3 Vdc.
- (d) Set channel switch to 108.00 MHz. The frequency shall be 520.5 MHz -50 ppm* (26.03 KHz).
- (e) The VCO voltage should not be less than 0.5 Vdc.
- (f) If the VCO voltages are out of tolerance at 117.9 and 108.00, set the channel switch to 117.90 MHz. Adjust L401 for 7.2 Vdc -0.3 Vdc.
- (g) Power Adjustment: Connect RF milliwattmeter to P401. Adjust L402 for 2.0 -0.5 mw across the band.
- * parts per million ie: Tolerance X Frequency = Hz50 X 575.0 = 28,750 Hz = 28.75 KHz

4.5.1.3 RF Transmitter Pulse Width Measurement and Adjustment

The transmitter pulse width is factory aligned and normally does not require field alignment. However, transmitter or modulator circuit problems that require the replacing of circuit components may necessitate a transmitter pulse width adjustment. The procedure for measurement and adjustment is given below:

- (a) Set the DME channel switch to 117.5 MHz.
- (b) Monitor the detected transmitter pulse pair on an oscilloscope.
- (c) Measure the transmitter pulse width at the 50% point of the pulses.
- (d) Pulse width should be 3.5 ± 0.5 us.
- (e) If adjustment is required, adjust width with R356 located on the main board.

4.5.1.4 Dead Time Measurement and Adjustment

- (a) Connect an oscilloscope to U312B-5.
- (b) Make the following settings on the DME Signal generator:
 - 1. Turn squitter off
 - 2. Set reply efficiency to 100%
 - 3. Set Mode Switch to "Range"
 - 4. Set Distance to 5 nm
 - 5. Set Attenuator to 78 dBm
 - 6. Turn IDENT off
 - 7. Trigger to "EXT".
- (c) Pulse width should be 60 us +15 -0 us.
- (d) If adjustment is required, adjust width with R347 located on the main board.

4.5.1.5 Display Intensity Adjustment

The maximum display intensity is set at the factory and should not require field adjustment. The pilot has a limited adjustment of the intensity through an access hole in the front panel. The alignment procedure is given below, but it is suggested that an alignment be performed only when a dissatisfaction with the maximum intensity has been expressed by the pilot.

- (a) Set R339, the pilot dim adjust, to midrange.
- (b) Connect a digital voltmeter to the base of Q316.
- (c) Using a black nontransparent material, block the light from the photocell, R378, and adjust R359 for -90 Vdc.
- (d) With the photocell still covered, check R339 dim adjust for display brightness variation. (It will only be slight).
- (e) Reset R339 to midrange.

4.5.1.6 Power Supply Checkout and Adjustment

The power supply check confirms operation of the switching regulator and DC/DC converter. The output of the switching regulator shall be 8.0 Vdc maximum and 7.2 Vdc minimum, and the output of the +14 volt line of the DC/DC converter shall be 14 -0.3 Vdc with an input of 14 or 28 volts. If not, connect a digital voltmeter to E601 and proceed as follows:

- (a) Note the value of the selected R608. Remove R608 from the circuit.
- (b) Connect a resistor test box across R609 set to the value of the removed R608.
- (c) Vary the resistance until a +14 -0.3 Vdc reading is obtained.
- (d) Check that the voltage at E602 is between 7.2 Vdc min to 8.0 Vdc max.
- (e) Solder an equivalent value resistor across R609.

4.5.2 RF Alignment

The alignment procedures are provided as a method of checking the tuning of RF circuits in the DME 890 after circuit components (RF transistors, capacitors) have been changed.

4.5.2.1 63 MHz IF Receiver Alignment

In the IF alignment, L704 through L709 are tuned by adjusting the coil's cores (slug), to provide a maximum detected pulse level.

The cores can be rotated for tuning, however, after tuning in and out for a peak many times, this excessive core movement will loosen the fit of the threads in the coil's body and thus the coil can become sensitive to vibration. If the core becomes loose, it should be removed, a single strand of lacing cord or equivalent inserted into the coils body and then replace the core (and adjust). Under no conditions should cement be used to secure the core.

Procedure:

- (a) Connect the DME 890 for a standard bench test.
- (b) Connect a scope probe to the collector of Q703. The cover over the top of the IF strip must be removed.
- (c) Set the DME Signal Generator output attenuator to produce a 1 volt peak-to-peak pulse pair.
- (d) Tune L704 through L709 and as the tuning progresses, reduce the DME Signal Generator's RF level to maintain a 1 volt peak-to-peak pulse pair.
- (e) Reinstall the cover.

4.5.2.2 RF Transmitter Exciter Alignment

If an RF transistor or capacitor has been changed in the transmitter, the following procedure should be used to check proper operation and realign the repaired stage.

NOTE: Either the DME 890's synthesizer, if operating properly, or an RF Signal Generator may be used. All steps using Generator are enclosed in parenthesis ().

- (a) Set DME 890 to 112.5 MHz. (Connect the RF Signal Generator to P102, set generator frequency to 550 MHz CW and output attenuator to +3 dBm.)
- (b) Using a 27K isolation resistor, connect a VTVM to the base of Q205 at resistor RT201.
- (c) If the exciter is working properly, the voltage will be approximately +0.2 Vdc.
- (d) Disconnect P102. (Reduce the Signal Generator level by 20 db.) The voltage should rise to +1 Vdc. This shows that stages Q1 through Q4 are operating correctly.
- (e) If one of the transistors, Q202 thru Q205 has been changed, the voltage in step "d" may be used to check alignment as follows:
 - 1. Set the DME 890 to 108.0 MHz.

 (Set the Signal Generator to 520 MHz at a +3 dBm level.)
 - 2. Observe the voltage at the base of Q205.
 - 3. Change the DME 890 frequency to 117.9 MHz. (Change the Signal Generator frequency to 575 MHz.)
 - 4. Observe the voltage at the base of Q205.
 - 5. Both voltage readings should be approximately 0.2 Vdc or slightly less.
 - 6. If at one frequency the voltage is considerably higher then the other, tune the coil associated with the changed component by spreading or compressing the coil.
 - 7. By this means it is possible to equalize the voltage at Q205 at both ends of the band.

4.6 TEST REQUIRED AFTER MODULE REPLACEMENT

The following are the recommended checks to perform after replacing a module in the DME 890. Only those checks pertaining to that module being replaced need be checked.

12/80

4.6.1 Gas Discharge Display Module

Display readings must be within tolerance. If not, recompensate per Section 4.5.1.6.

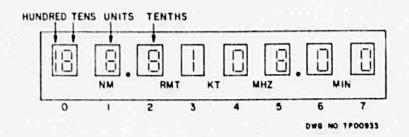


FIGURE 4-6. DISPLAY

- (a) Set DME 890 Mode Switch to "FREQ" position.
- (b) Set DME Generator and DME 890 to 108.0 MHz.
- (c) Set DME Generator Mode Switch to "RANGE".
- (d) Set DME Distance to 0.1 nm, check digit #2 (tenths) for 0-9 capability. (NOTE 1)
- (e) Set DME Distance to 1.0 nm, check digit #1 (units) for 0-9 capability. (NOTE 1)
- (f) Set DME Distance to 10.0 nm, check digit #0 (tens) for 0-9 capability. (NOTE 1)
- (g) Set DME Distance to 110.0 nm, check digit #0 (hundred) for the numeral "1".
- (h) Check bars in digits 0, 1, 2, by setting generator to 200 nm.
- (i) Check digits #3, #4, #5, #6, #7 by channeling the DME 890 from 108.0- to 117.95 MHz.

NOTE 1: Rechannel the DME after each distance change.

4.6.2 Power Supply Module

- (a) Check for +14 0.3 Vdc at E601.
- (b) Check for +7.2 to 8.0 Vdc at E602.

4.6.3 63 MHz IF Receiver Module.

After replacing this module check "lock-on" sensitivity at high and low frequencies. It should be -82 dBm minimum. If this sensitivity checks OK, unit is operating properly. If lock-on is less than -82 dBm, listen to IDENT, adjust RF level if noisy. Retune IF coils L704 thru L709 for maximum IDENT volume.

4.6.4 Transmitter Module

Check only for proper pulse width and power output. If defective, return it to the factory for exchange.

TRANSMITTER OUTPUT AND RECEIVER SENSITIVITY CHECK

- Set the DME Generator to 108,00 MHz and -86 dBm level. Check the following while channeling the unit from 108.00 to 108.50 by KHz, 108.50 to 117.50 MHz by MHz, and 117.5 to 117.90 by KHz:
 - Minimum transmitter power to be 22 watts

2. Standard transmitter pulse shape

3. Transmitt pedestal NOT to exceed 10% of pulse amplitude

4. Receiver sensitivity -82 dBm or less

5.

PRF meter reading of 25 to 30 Hz Pulse spacing of 12 $\stackrel{+}{-}$.1 us on X channels, 36 $\stackrel{+}{-}$.1 us on Y channels

Pulse width at 50% point shall be $3.5 \pm .5$ us 7.

Audio output: Set generator 20 dB above minimum lock-8. on sensitivity and check audio output. Nominal 5 mw into a 600 ohm load.

4.7.1 Range, Velocity, and Time-To-Station Check

Set the DME generator to -72 dBm, range to 60 miles:

- The DME shall read $60.0 \pm .2$ miles, change setting to -82 dBm. Reading shall be within -. 1 miles of that observed in step "a".
- Increase generator to -10 dBm, distance shall not change (b) by more than -. 1 mile of the reading observed in step "a".

(c) Set RF level to -78 dBm.

- (d) Check memory time by setting the generator's IDENT to 1350. The distance shall remain for 6 seconds (minimum) and bar before 15 seconds. Turn generator's IDENT off.
- Şet the distance to 000.0 miles. All readings shall be (e) -0.2 miles (RF level at -78 dBm).
 - Rotate the tenths mile dial through all 10 positions. Leave dial in .0 position
 - Repeat for units, and tens
 - 3. Set the hundreds dial to 1
 - Set the hundreds dial to 2.
- Set the generator's distance/velocity switch to velocity, (f) the RF level to -72 dBm, the velocity to 100 KTs, and the IN/OUT switch to outbound.
- Turn the DME 890 off for 5 seconds then turn it on and (g) observe: within 3 minutes the ground speed display shall read between 95 and 105 KTs.
- Change generator's velocity to 360 KTs and reverse the direction (to inbound). Within 4 minutes the ground speed must read between 342 and 378 KTs.
- Change generator's velocity to 60 KTs, within 4 minutes the (i) ground speed must read between 55 and 65 KTs.

4.8 WAVEFORMS

Waveforms and test locations are identified on the schematics in Section 6 by means of a reference number in a diamond-shape enclosure. These waveforms are also referenced in the trouble-shooting flow charts Figures 4-8 thru 4-14.

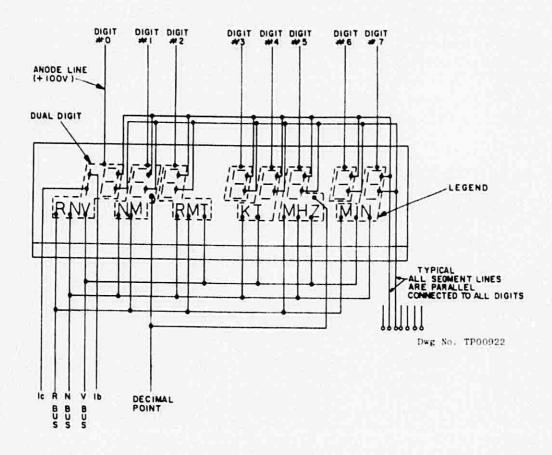


FIGURE 4-7. GAS DISCHARGE DISPLAY INTERNAL WIRING

MAINTENANCE SECTION 4

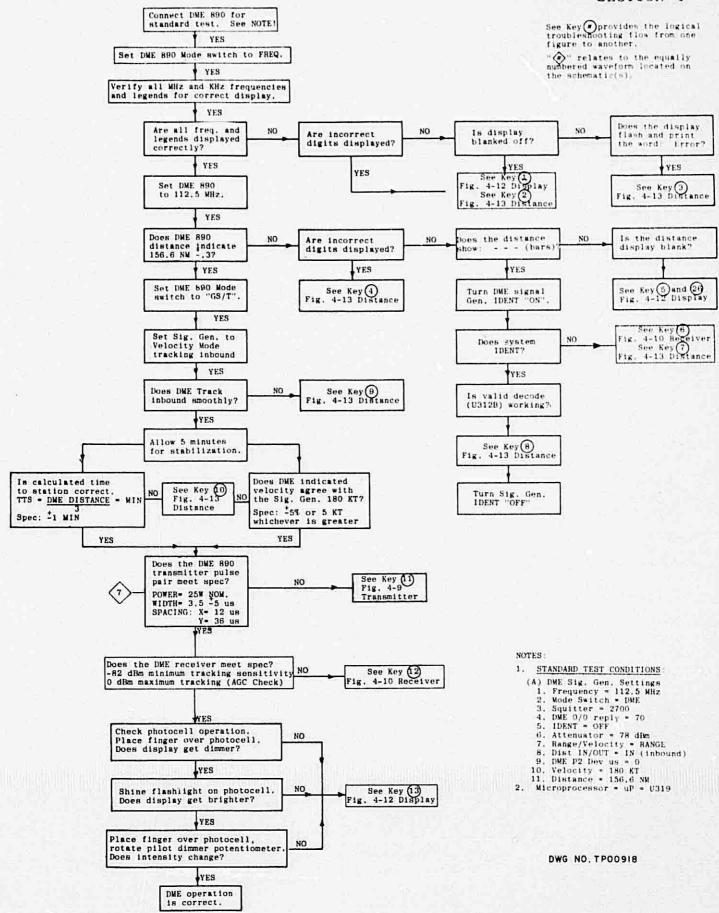
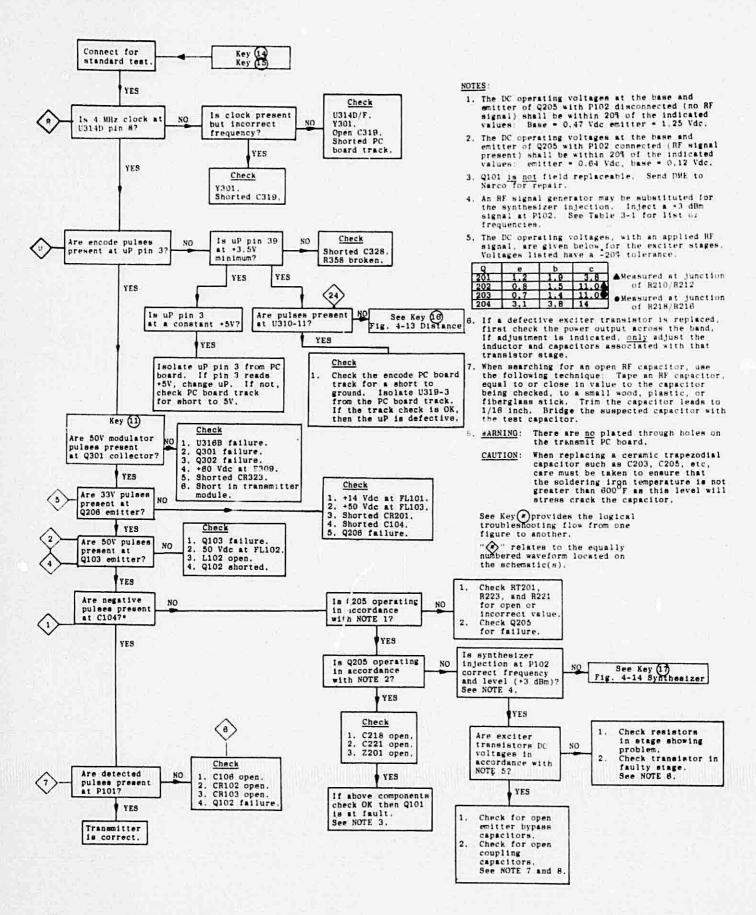


FIGURE 4-8. FUNCTIONAL CHECKOUT FLOW CHART



DWG. NO TP00919

FIGURE 4-9. TRANSMITTER TROUBLE ISOLATION FLOW CHART

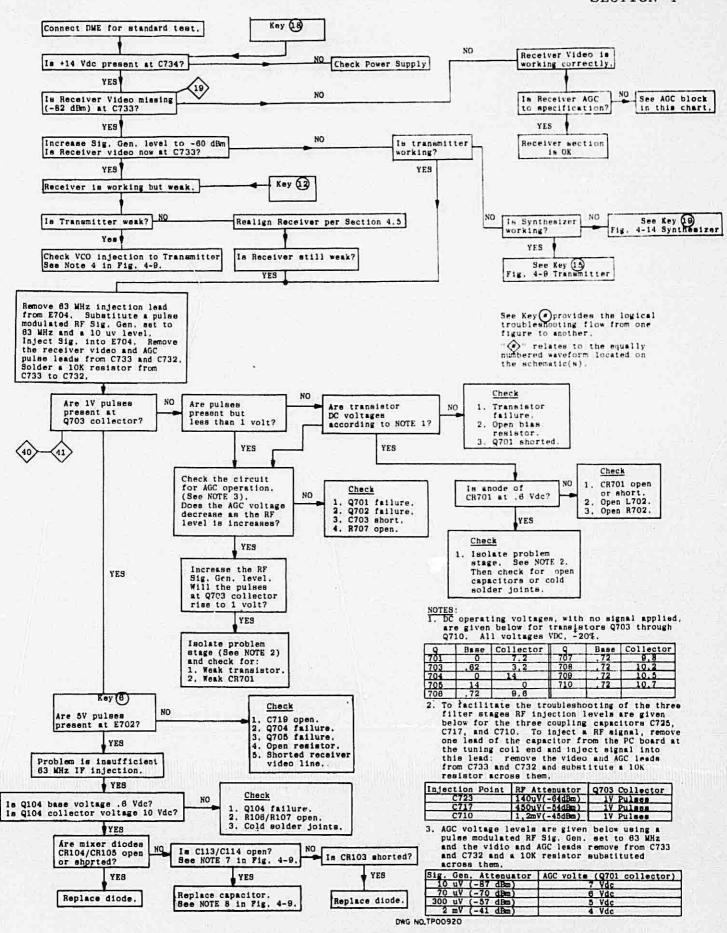


FIGURE 4-10. RECEIVER TROUBLE ISOLATION FLOW CHART

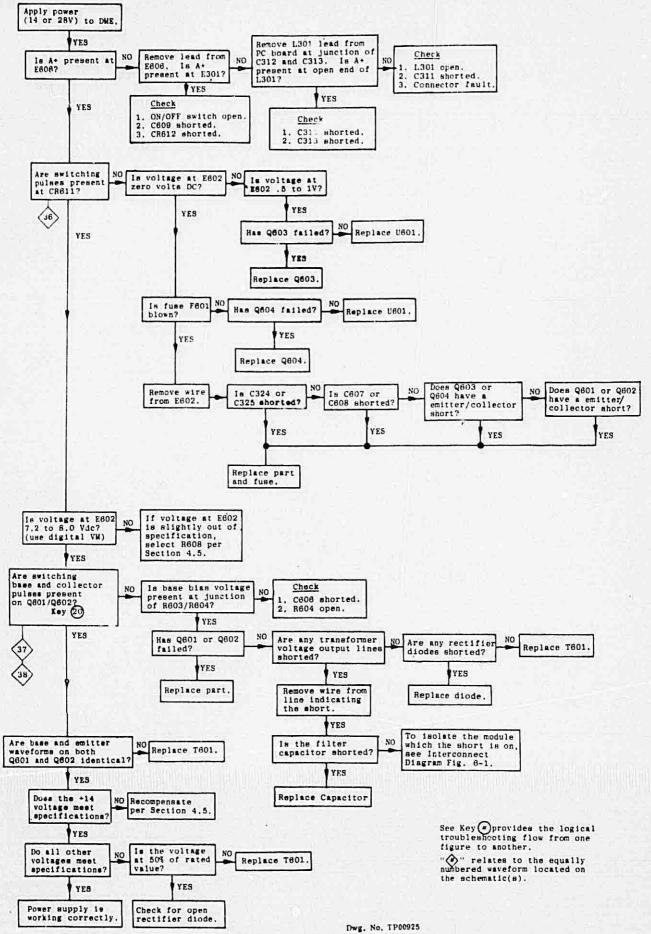


FIGURE 4-11. POWER SUPPLY TROUBLE ISOLATION FLOW CHART

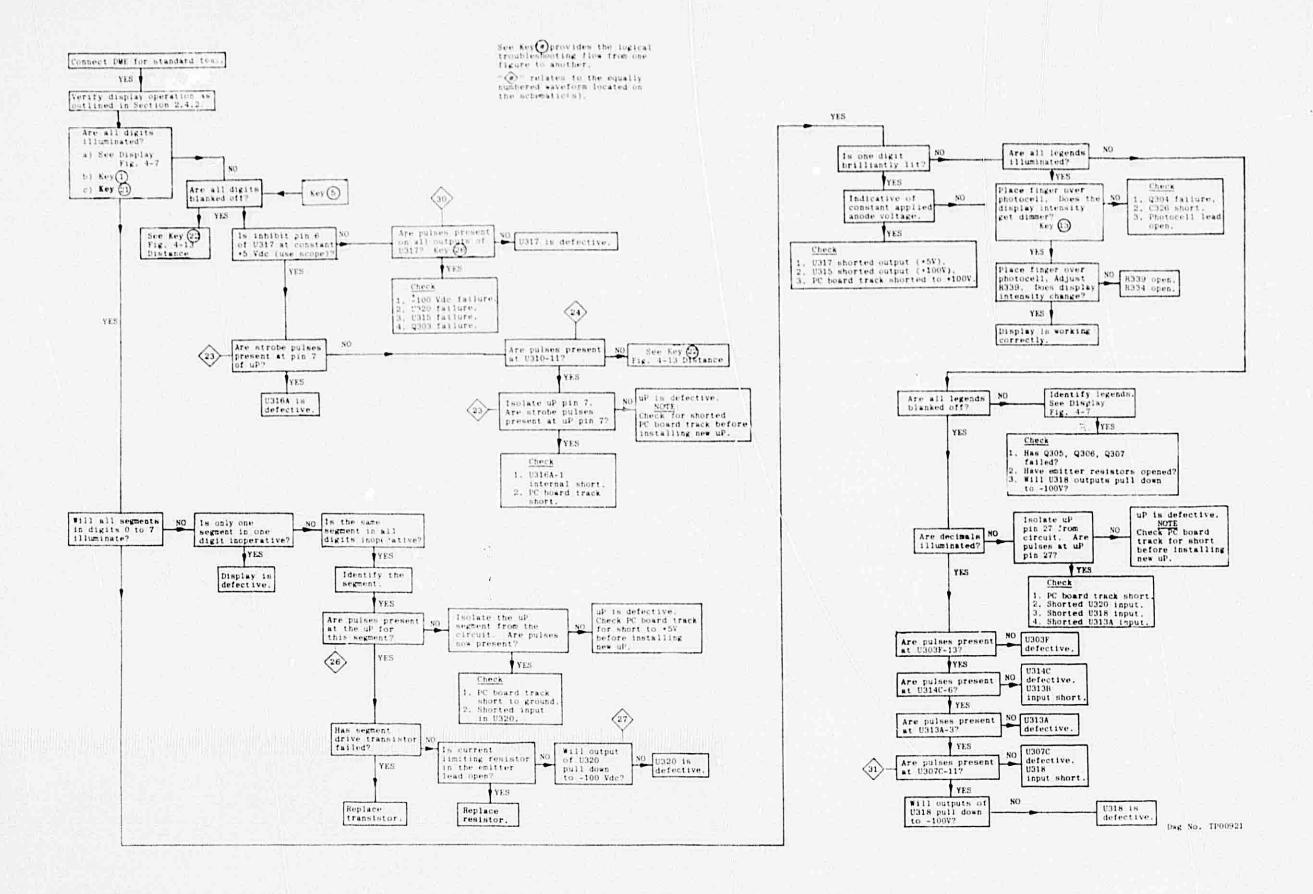


FIGURE 4-12. DISPLAY TROUBLE ISOLATION FLOW CHART (sheet 1 of 2)

4-21

(4-22 Blank)

SEE BLOW-UP

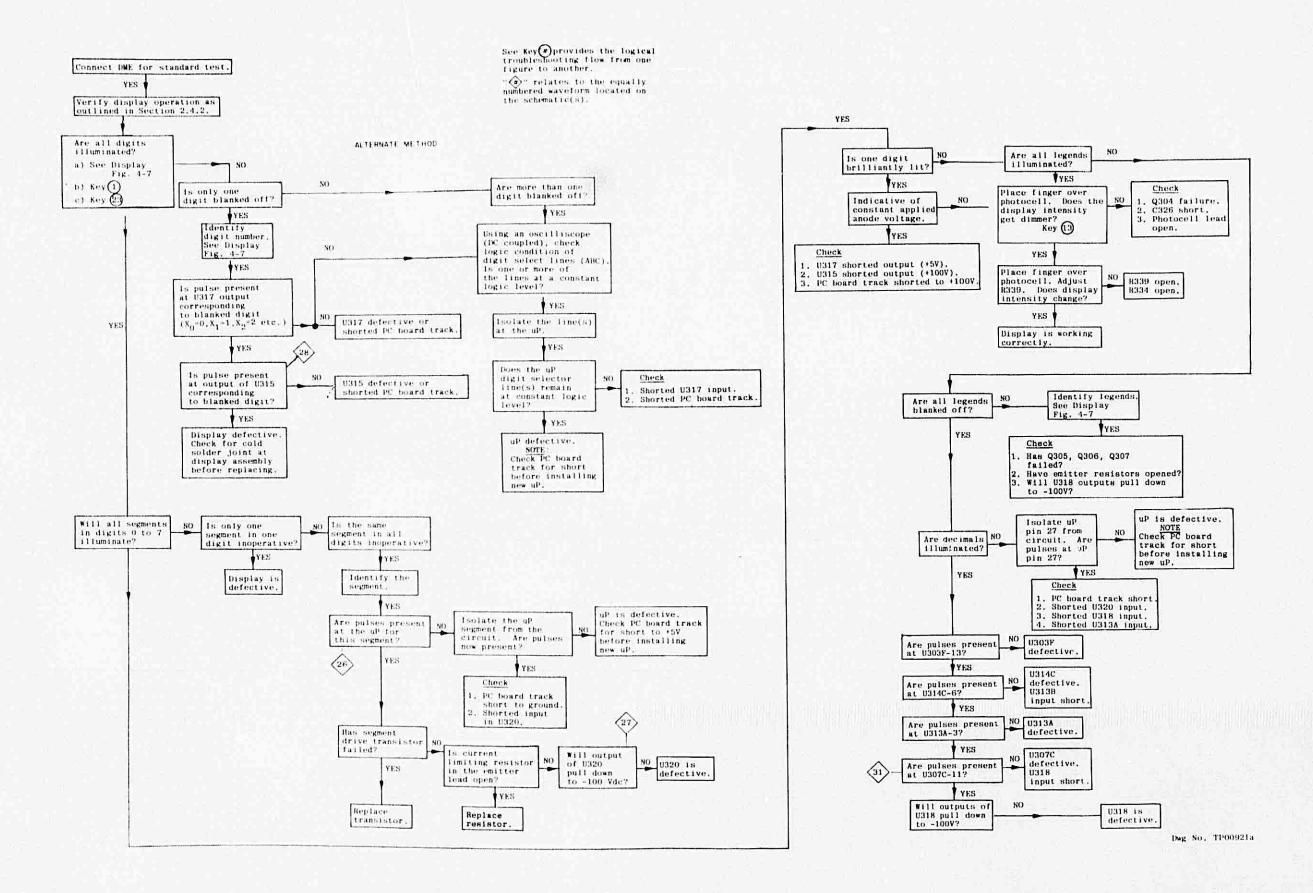
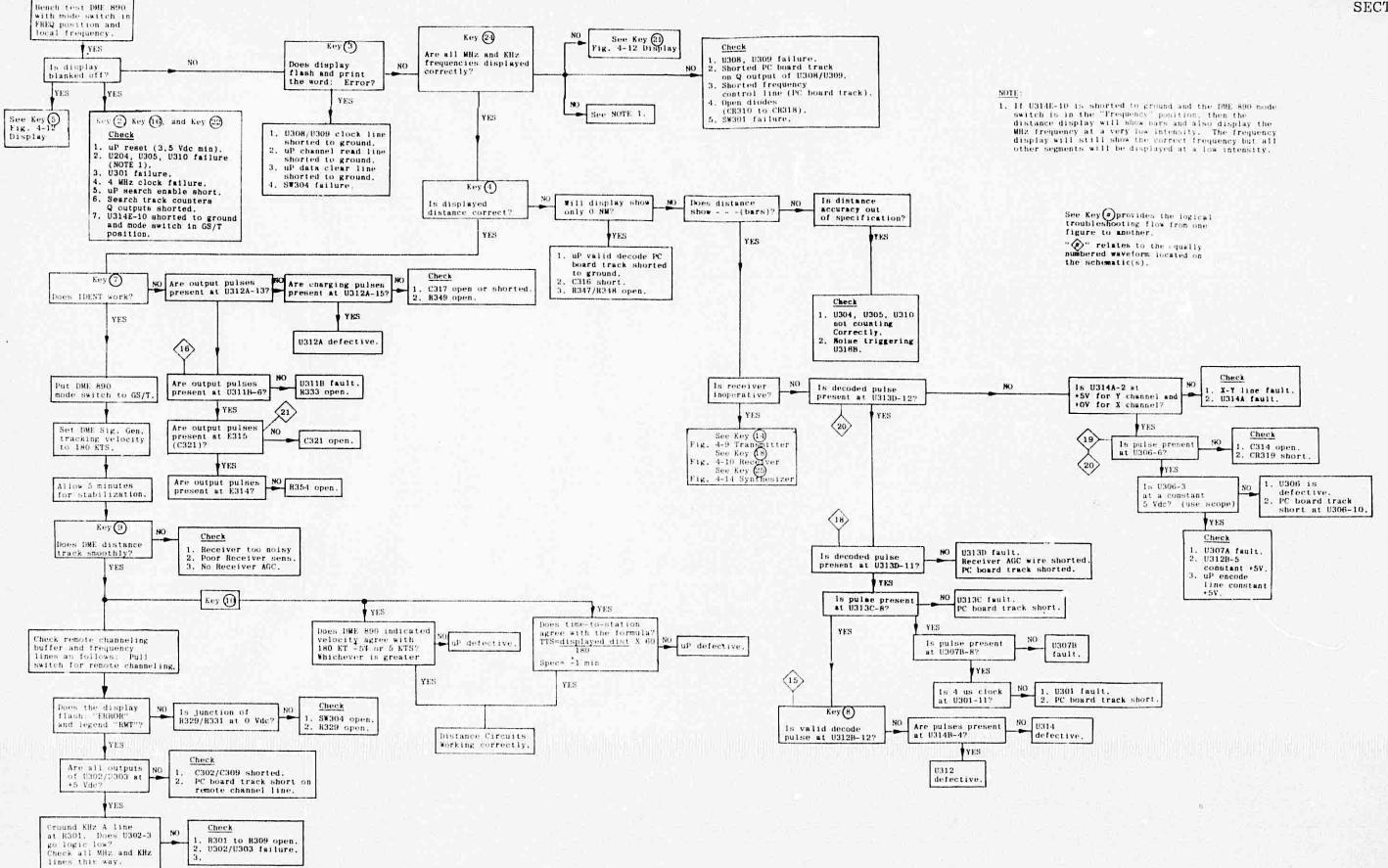


FIGURE 4-12. DISPLAY TROUBLE ISOLATION FLOW CHART ALTERNATE METHOD (sheet 2 of 2)

4-23



YES

DWG NO 1P00923

Remote channel circuits are correct.

FIGURE 4-13. DISTANCE, FREQUENCY, IDENT, AND REMOTE CHANNEL ISOLATION FLOW CHART

4-25 (4-26 Blank)

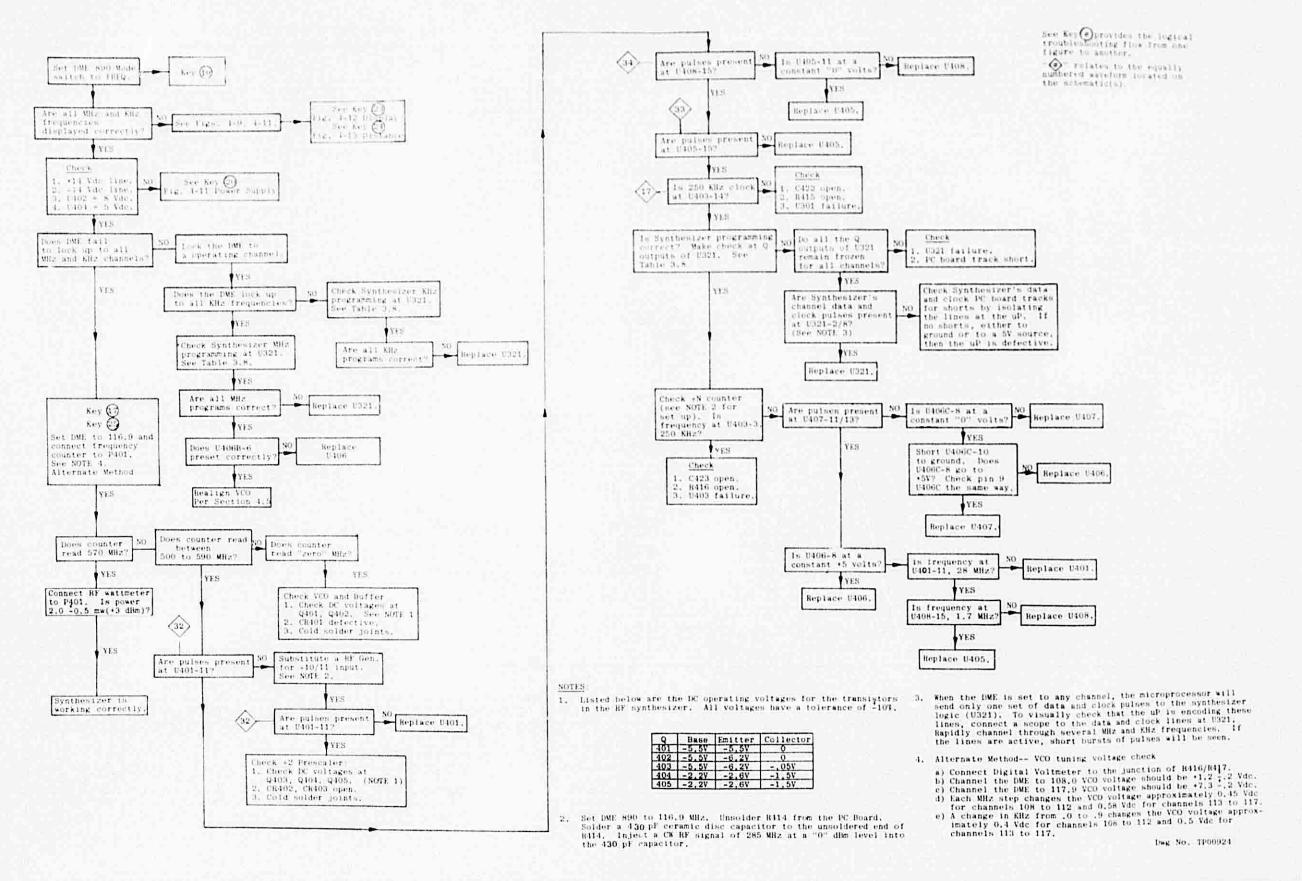


FIGURE 4-14. SYNTHESIZER ISOLATION FLOW CHART

DME 890

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5.1 GENERAL

This Section provides simplified exploded view drawings of the DME 890.

The lists represent a complete hypothetical complete disassembly of the Unit. Parts that are attached by hardware are related to that hardware by being listed following the words ATTACHING PARTS. The symbol - - - * - - - designates the ending of that set of hardware.

Only those electrical parts that are related to mechanical parts are listed to show their relationship, all remaining electrical parts will be found in the Electrical Parts List on the reverse side of the schematic in Section 6.

Before attempting any disassembly review the exploded views, to provide foresight - disassemble only those parts required to be removed.

The lists present piece parts individually. At times such individual parts are not available as they are assembled into process assemblies for future assembly. The reason for this is because, in most cases, special fixtures are required to do the job properly. When ordering any mechanical part please identify it by part number and relate it to its figure and item number.

5.2 MODULES

Narco has added the DME 890's three replacement modules to its module replacement program. The modules are available for your stock, ready when the need calls. The object of the program is obvious - to provide fast customer service.

Replacement modules may be ordered by using their complete and tested replacement module part number.

MODULE	ORDER NO.
IF Receiver	01375-1390
Transmitter	01376-1390
Power Supply Assy	01379-1390

DME 890 MECHANICAL PARTS LIST

Fig. and Index	Part Number	Symbol Number	Description Q	ty
5.1	01380-0101		DME 890	1
-1	04912-0001		LABEL, Nameplate	1
-2	04920-0001		LABEL, Modification	1
-3	04911-0001		LABEL, Warranty Identification	1
-4	50217-0001		COVER, Top	7.5
Ш	00000 0501		(ATTACHING PARTS)	
-5	82869-0701		SCREW, Mach, Taptite, SS, Phil Hd, 4-40 X 3/16	
			4-40 X 5/10	= :
-6	50217-0001		COVER, Bottom	
			(ATTACHING PARTS)	
-7	82869-0701		SCREW, Mach, Taptite, SS, Phil Hd,	
			4-40 X 3/16	
	00000 0001		*	
	83038-0001	7001 /7000	INSULATOR, Phenolic	
	11454-0003 84540-0001	Z801/Z806	BEAD, Ferrite GASKET, 9 inches long (EMI/RFI)	
	01377-0101		TOP FRAME ASSY (See Figure 5.2	
-11	01377-0101		for breakdown)	
			(ATTACHING PARTS)	
-12	82892-0402		SCREW, Mach, SS, Phil Hd,	
			4-40 X 3/16	
-13	84536-0702		SCREW, Mach, SS, Phil Hd,	
			4-40 X 3/16	
-14	82802-0703		WASHER, Lock, Int. Tooth, SS,	
			NO. 4	
_15	88238-0001		KNOB, .128 OD X .46 lg (KHz)	
-10	00200-0001		(ATTACHING PARTS)	
-16	82863-0718		SETSCREW, 4 flutes, SS, 4-40 X 1/8	5
1.0	02000 0.20		*	
-17	88237-0001		KNOB, .255 OD X .46 lg (MHz)	
			(ATTACHING PARTS)	
-18	82863-0718		SETSCREW, 4 flutes, SS, 4-40 X 1/8	,
10	50044 0111		DANEL Train	
-19	50244-0111		PANEL, Trim (ATTACHING PARTS)	
-20	82809-0306		SCREW, Mach, Black, Nylon, Flat Hd	١.
-20	02000 0000		4-40 X 7/16	,
			*_1 1 1 1 1	
-21	50276-0001		SHIELD, Toggle Switch	
	50277-0001		SHIELD, Switch Support	
-23	01379-0101		POWER SUPPLY AND RIGHT SIDE PANEL	
			(See Figure 5-5 for	
			breakdown)	

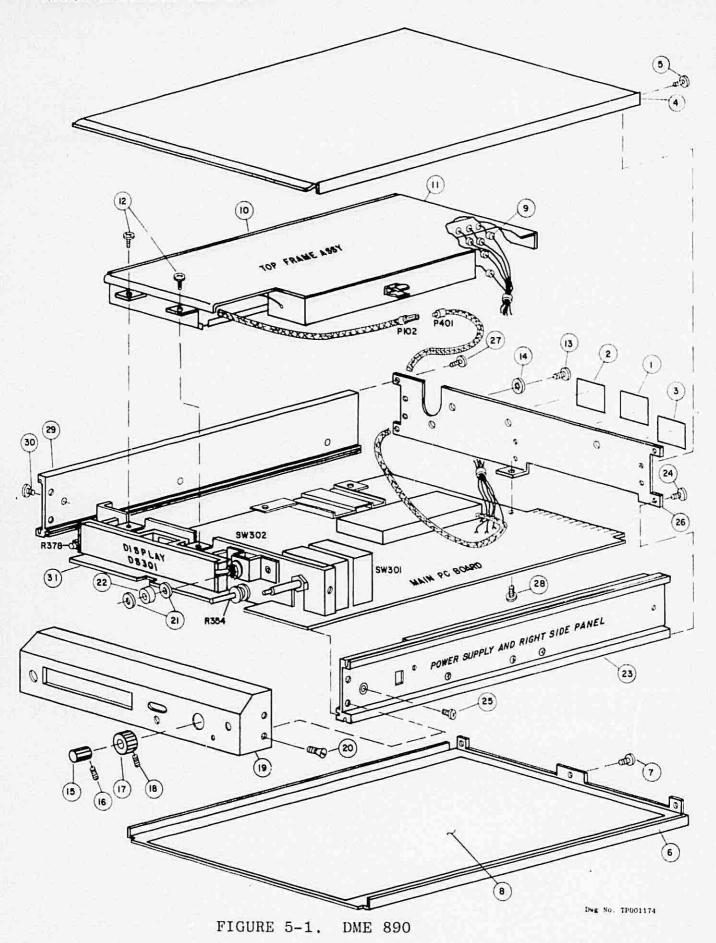


Fig and Index	Part Number	Symbol Number	Description	Qt	y
				1	_
-			(ATTACHING PARTS)		
-24	84537-0702		SCREW, Mach, Taptite, SS, Phil		
			Undercut, 4-40 X 3/16		2
-25	82869-0704		SCREW, Mach, Taptite, SS, Phil		
			4-40 X 3/8		1.
			*		
-26	50205-0002		PLATE, Rear	1	1
			(ATTACHING PARTS)		
-27	82869-0704		SCREW, Mach, Taptite, SS, Phil		
			4-40 X 3/8		2
-28	82869-0704		SCREW, Mach, Taptite, SS, Phil	Hd,	
			4-40 X 1/4		1
			*		
-29	50015-0101		PANEL, Left Side		1
			(ATTACHING PARTS)		
-30	82884-0504		SCREW, Mach, SS, Phil Hd,		
			4-40 X 5/16		2
			*		
-31	01378-0101		MAIN PC BOARD (See Figure 5-6	for	
			breakdown)		1

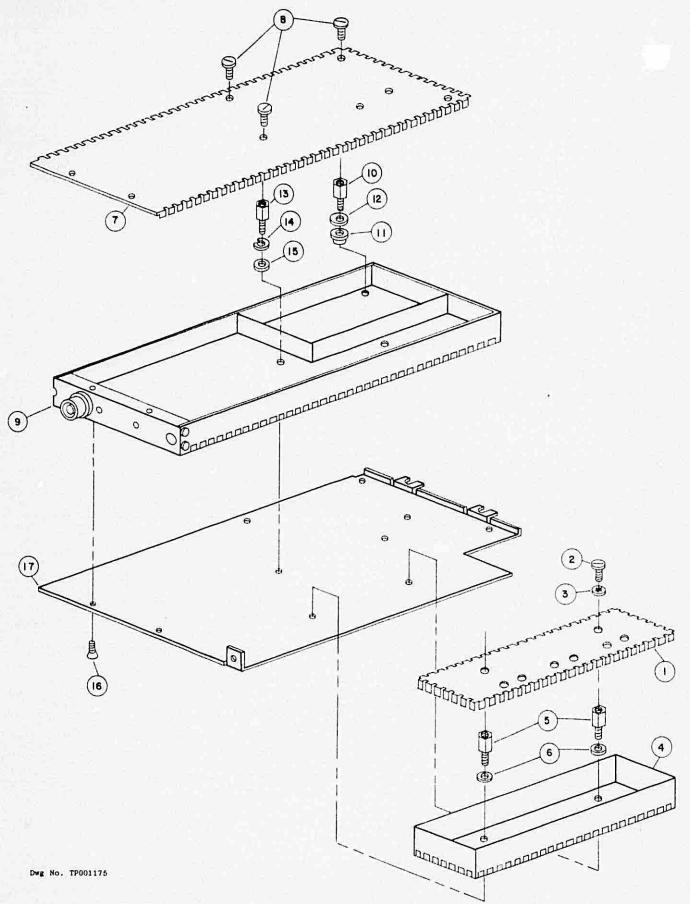


FIGURE 5-2. TOP FRAME ASSEMBLY

Fig. and Index	Part Number	Symbol Number	Description	Qty
5.2	01377-0101		TOP FRAME ASSEMBLY (See Figure	
			5.1-11 for next higher assembly)	Ref
-1	See Item 4		COVER, IF Receiver (part of	
	200 200 2		IF Receiver Assy)	_
			(ATTACHING PARTS)	
-2	82892-0402		SCREW, Mach, S1, Pan Hd,	•
- 1			4-40 X 3/16	2 2
-3	82802-0703		WASHER, Lock, Int. Tooth, No. 4	4
-4	01375-0101		RECEIVER, IF ASSY (See Figure	
	01373-0101		5.3 for breakdown)	1
			(ATTACHING PARTS)	
-5	81342-0011		SPACER, Threaded, 4-40,	
			.500 lg Hex body	2
-6	81312-0016		WASHER, Spring	2
	reconstruction		*	
-7	See Item 9		COVER, (Part of Trans/Mod/	
			Presel/Recv Mixer)	
-8	82892-0402		(ATTACHING PARTS) SCREW, Mach, S1, Pan Hd,	
-0	02092-0402		4-40 X 3/16	6
			*	
-9	01376-0101		TRANSMITTER/MODULATOR/	
			PRESELECTOR/RECEIVER MIXER	
			ASSY (See Figure 5.4 for	
			breakdown)	1
1 1			(ATTACHING PARTS)	
-10	81342-0012		SPACER, Threaded, 4-40, .437 lg Hex body	3
111	81810-0001		WASHER, Shoulder	3
	81312-0016		WASHER, Spring	3
	8 81342-0013		SPACER, Threaded, 4-40,	
			.375 lg Hex body	3
-14	82969-0004		WASHER, Lock, Split, No. 4	3
	81312-0016		WASHER, Spring	3
-16	8 84532-0702		SCREW, Mach, Phillips, Flat Hd,	0
			2-56 X 3/16	2
	7 50006 0101		PLATE, Mounting	1
-17	7 50026-0101		PINIE, MOUNTING	-

- NOTES: 1. IF Receiver Subassy (items 1 thru 6) available as a tested subassy Order No. 01375-1390.
 - 2. Transmitter/Modulator/Preselector/Receiver Mixer Assy available as a tested subassy includes items 7 thru 17. Order No. 01376-1390.

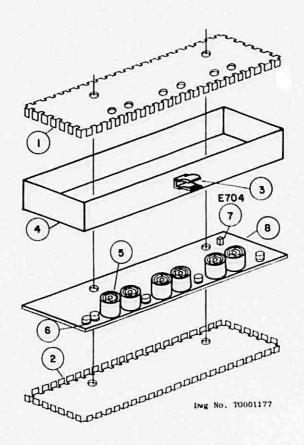
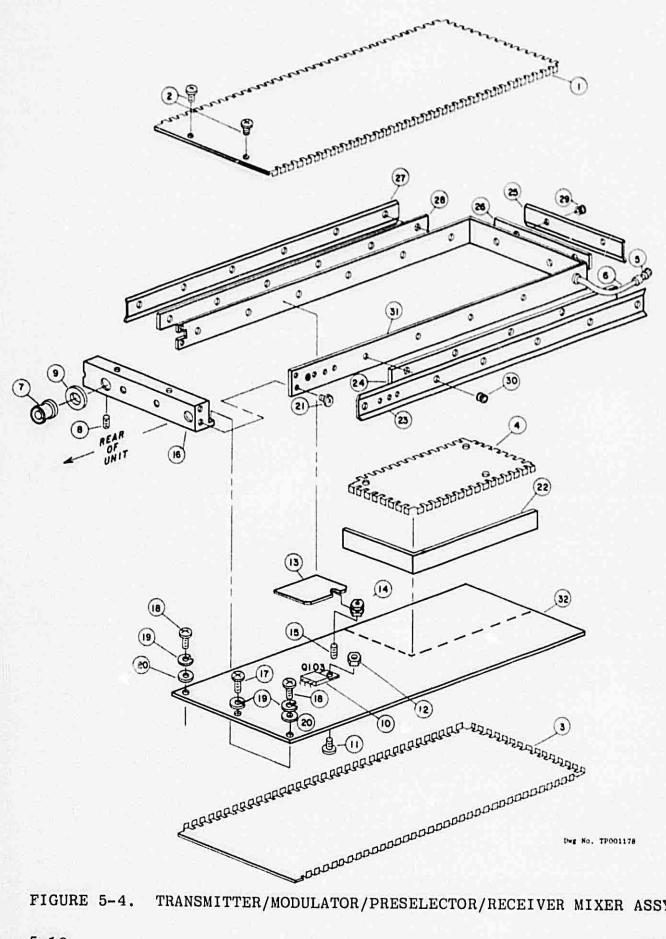


FIGURE 5-3. IF RECEIVER ASSEMBLY

DME 890 MECHANICAL PARTS LIST

Fig. and Index	Part Number	Symbol Number I	Description	Qty
5.3	01375-0101	1	RECEIVER, IF ASSY (See Figure 5- item 4 for next higher	-2,
			assembly)	Ref
1 21	50022-0001		COVER, Top	1
	50022-0002		COVER, Bottom	1
	84047-0003		CRADLE, Mount (P401/P402)	1 1
	50021-0001		SHIELD, Wraparound	ī
-5	50038-0001		SHIELD, Can, IF coil (L704-	
			L709	6
-6	83037-0002		PAD, Transistor Mounting	
			Q706-Q710	5 1
	81808-0104		TERMINAL, Square Post	1
-8	50027-0001		PC BOARD (Less Components)	NP
		NOTES:	1. NP - Non-Procureable	
			2. See List 5-2's Note 1 for	
			replacement module part nu	umber.

Fig. and Index	Part Number	Symbol Number	Description	Qty
5.4	01376-0101		TRANSMITTER/MODULATOR/PRESELECTOR/ RECEIVER MIXER ASSY (See Figure 5.2, item -9 for next higher assembly)	Ref
-1	50020-0001		COVER, Trans (Top) (ATTACHING PARTS)	1
-2	84533-0702		SCREW, Mach, SS, Phillips Hd, 2-56 X 3/16	2
-3	50020-0002		COVER, Bottom	1
-4	50019-0001		COVER, Exciter	1
	41244-0001	P102	CONNECTOR, Plug	1
		P102	COAX CABLE, Double Shielded 7"	1
	90078-0001	D1 01		1
	41318-0001	P101	CONNECTOR, Coax, BNC, Female	1
	82863-0718		SETSCREW, 4 Flutes, 4-40 X 1/8	1
-9	81213-0139		SPACER, A1, .500 OD X .390 ID X .070 lg	1
	==000 000=	0100	mpayoromon Danlington	1
-10	75638-0007	Q103	TRANSISTOR, Darlington (ATTACHING PARTS)	
_11	82888-0003		SCREW, Pan Hd, Nylon, 4-40 X 1/4	1
	82925-0001		NUT, Hex, Nylon 4-40	1
-13	50049-0001		PLATE, Coupling	1
	88239-0001		KNOB, Tuning Adjust	1 1
			(ATTACHING PARTS)	
-15	82813-0006		SCREW, Mach, Bind Hd, 2-56 X 7/16	1
			* =	
1.6	50025-0001		SUPPORT, Rear	1
-10	30023-0001		(ATTACHING PARTS)	-
17	04522 0702		SCREW, Mach, SS, Phillips Hd,	
-11	84533-0702		2-56 X 3/16	1
	04500 0500		SCREW, Mach, SS, Phillips Hd,	1.
-18	84533-0703			2
1 2 2 2			2-56 X 1/4	3
	82969-0002		WASHER, Lock, Split, No. 2	2
	81810-0002		WASHER, Shoulder	4
-21	84533-0702		SCREW, Mach, SS, Phillips Hd, 2-56 X 3/16	4
			GUIELD Internal Support	1
	50018-0001		SHIELD, Internal Support	1
-23	50051-0002		CLIP, Spring, 9 inches long	4
			(w/filter holes)	1
-24	50050-0001		SPACER, (Spring Clip)7+ inches	-
			long	1
-25	5 50051-0003		CLIP, Spring, 2.5 inches long	
			(rear)	1



TRANSMITTER/MODULATOR/PRESELECTOR/RECEIVER MIXER ASSY FIGURE 5-4.

Fig. and Index	Part Number	Symbo: Number		Qty
-26	50050-0003		SPACER, (Spring Clip) 2.5	1
97	50051-0001		CLIP, Spring, 9 inches long	1
	50050-0002		SPACER (Spring Clip) 9 inches	3
-20	30030-0002		long (ATTACHING PARTS)	1
00	01054 0027		EYELET	1
	81254-0037 81254-0033		EYELET	13
-30	81234-0033		*	
91	50017-0001		SHIELD, Wraparound	1
			PC BOARD (Less Components)	NP
-32	50012-0001		PC BOARD (Less components)	
			ITEMS NOT SHOWN	
	83011-0014		INSULATOR, GLASS EPOXY,	
	00011-0014		1-1/16 X 7/16 with hole	1
	84540-0001		GASKETING, EMI/RFI, 2-3/4 inch	1
	90039-0014		STRIP, Electrical, 3/8 long X	
	50035-0014		3/32 wide X .005, Silver	2
	NOTES	2.	NP - Non-Procureable See List 5-2's Note 2 for replacement module part number.	

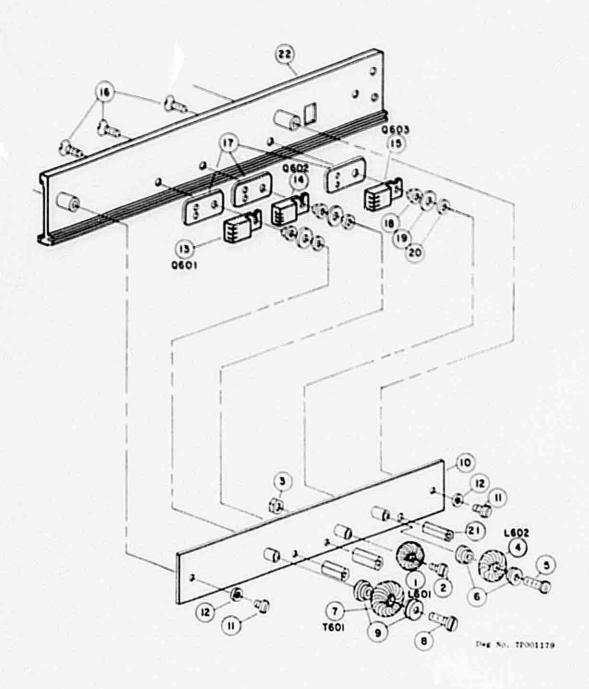


FIGURE 5-5. POWER SUPPLY AND RIGHT SIDE PANEL

Fig. and Index	Part Number	Symbol Number	Description	Qty
5.5	01379-0101		POWER SUPPLY AND RIGHT SIDE PANEL (See Figure 5-1, item -23 for next higher assembly)	Ref
-1	11879-0001	L601	CHOKE, Toroid (ATTACHING PARTS)	1
-2	82888-0009		SCREW, Nylon, Bind Hd, 4-40 X 3/4	1
-3	82925-0001		NUT, Hex, Nylon, 4-40	1
-4	11880-0001	L602	CHOKE, Toroid (ATTACHING PARTS)	1
-5	84536-0709		SCREW, Mach, Phil Hd, 4-40 X 3/4	1
-6	81335-0019		INSULATOR, Shoulder	2
-7	11933-0001		TRANSFORMER, DC to DC (ATTACHING PARTS)	1
-8	84536-0709		SCREW, Mach, Phil Hd, 4-40 X 3/4	1
-9	91335-0019		INSULATOR, Shoulder	2
-10	50011-0101		PC BOARD (Less Components) (ATTACHING PARTS)	NI
-11	84536-0703		SCREW, Mach, Phil Hd, 4-40 X 1/4	2
-12	82802-0703		WASHER, Lock, Internal Tooth No. 4	2
-13	75625-0001	Q601	TRANSISTOR, Silicon, PNP, 2N6109	1
-14	75625-0001	Q602	TRANSISTOR, Silicon, PNP, 2N6109	1
-15	75659-0002	Q603	TRANSISTOR, Silicon, NPN, TIP31A	1
			(ATTACHING PARTS)	
-16	82884-0507		SCREW, Mach, Flat Hd, Undercut 4-40 X 1/2	3
-17	83031-0003		INSULATOR, Transistor	3
	8 81335-0012		INSULATOR, Shoulder	3
	81307-0123		WASHER, Flat, Al, .187 OD X	
-			.116 ID X .025 thk	3
-20	82969-0004		WASHER, Lock, Split, No. 4	3
	81207-0075		SPACER, Hex, Threaded thru, 4-40 (Nut)	3
-29	2 50016-0101		PANEL, Right Side	1

NOTE: Power Supply and Right Side Panel available as a tested subassy Order No. 01379-1390.

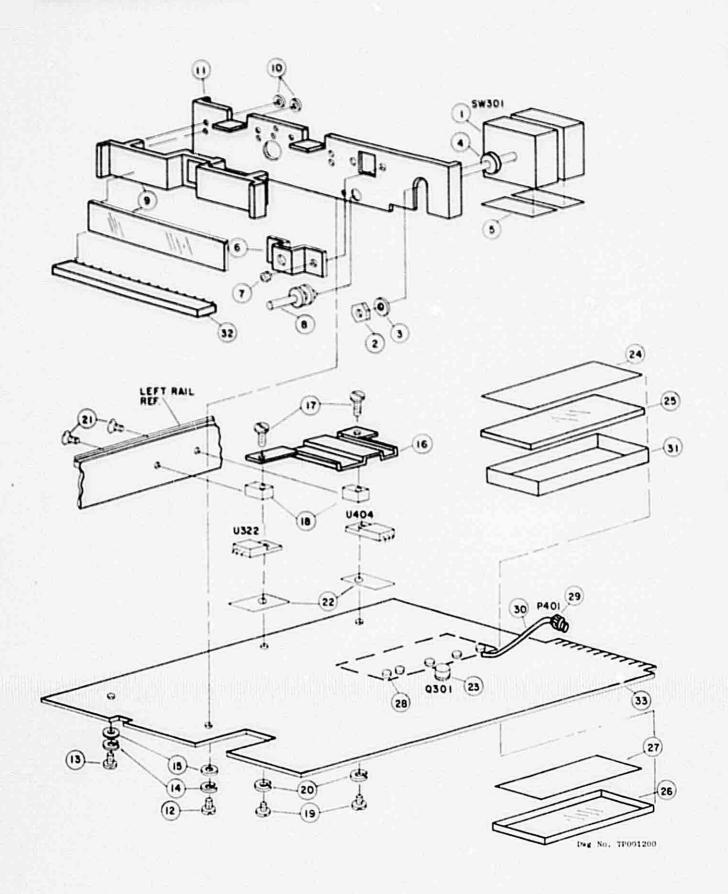


FIGURE 5-6. MAIN PC BOARD

Fig. and Index	Part Number	Symbol Number	Description	Qty
5.6	01378-0101		MAIN PC BOARD (See Figure 5-1, item -31 for next higher assembly)	Ref
-1	61658-0001	SW301	SWITCH, Frequency (ATTACHING PARTS)	1
-2	82900-0723		NUT, Hex, S/S, 3/8-32	1
	82802-0735		WASHER, Lock, Int Tooth, 3/8	1
-4	81213-0137		SPACER, A1, .390 ID X .500 OD X .070 lg	1
-5	99065-0004		TAPE, Double Sided	1
-6	50216-0001		BRACKET, Switch (SW302) (ATTACHING PARTS)	1
-7	81254-0002		EYELET	2
-8	50242-0001		KNOB, ON-OFF-Vol- IDENT	1
-9	50014-0001		DISPLAY, Gas Discharge (ATTACHING PARTS)	1
-10	81297-0011		RING, Retaining, Self-locking	8
-11	50223-0001		SUPPORT, Display (ATTACHING PARTS)	1
-12	82869-0702		SCREW, Taptite, S/S, Pan Hd, 4-40 X 1/4	1
-13	82869-0703		SCREW, Taptite, S/S, Pan Hd, 4-40 X 5/16	1
-14	82969-0004		WASHER, Lock, Split, S/S, No. 4	2 2
0.00	81307-0086		WASHER, Flat, Special	2
-16	50040-0001		HEATSINK (IC) (ATTACHING PARTS)	1
-17	84536-0703		SCREW, Mach, Pan Hd, S/S, 4-40 X 1/4	2
-18	50039-0001		HEATSINK (U322/U404) (ATTACHING PARTS)	2
-19	84536-0703		SCREW, Mach, Pan Hd, S/S, 4-40 X 1/4	2
-20	82969-0004		WASHER, Lock, Split, S/S, No. 4	2
	82884-0502		SCREW, Mach, Flat Hd, Undercut, 4-40 X 3/16	2
-22	83040-0001		INSULATOR, Phenolic	2

DME 890 MECHANICAL PARTS LIST

Fig. and Index	Part Number	Symbol Number	Description	Qty
-23	52726-0001		TRANSIPAD (Q301)	1
The second secon	83038-0002		INSULATOR, Phenolic	1
	50024-0001		COVER, (Synthesizer -	
			Component side)	1
-26	50047-0001		COVER, (Synthesizer -	
			Circuit side)	1
-27	83038-0002		INSULATOR, Phenolic	1
-28	83037-0003		PAD, Transistor (Q401/Q405)	5
-29	41244-0002	P401	CONNECTOR, Male	1
-30	90078-0001		COAX CABLE, Double Shielded	1
-31	50023-0001		SHIELD, Wraparound	1
-32	50231-0001	J302	CONNECTOR, Elsulay	1
-33	50009-0001		PC BOARD (Les, Components)	NP

NP - Non-Procureable

NARCO AVIONICS DME 890

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6.1 GENERAL

This Section contains a set of Schematics and support information for the DME 890. Such support information comprises:

- An internal interconnect diagram
- Component location drawings with "solder track"
- Voltage test points
- Waveforms
- Electrical Parts List on the reverse side of the schematic

6.1.1 Internal Interconnect Diagram

Figure 6-1, the internal interconnect diagram shows point-to-point wiring. This figure's To/From Wiring List is a redundant list, that is, the left column contains, in alphanumeric sequence, both ends of a lead, allowing one to find the opposite end of a lead quickly. Lead functions and wire colors are given. (Note: wire colors may be changed without notice).

6.1.2 Component Location Drawings

The component drawing adjacent to its schematic is provided to give quick schematic/unit orientation. The PC runs shown are provided to aid in tracing and identifying components. Numerous waveform and voltages are shown on or about the schematic to allow quick troubleshooting, in conjunction with the trouble isolation flow charts of Section 4.

6.1.3 Electrical Parts List

The Electrical Parts List, formerly located in Section 5 will be found on the reverse side of its schematic. The parts listed are those parts found in the schematic,

This list contains such data as: the parts effectivity, and an Action if any, its electrical symbol number, Narco Part Number, Description, and its component assembly and schematic grid coordinates.

6.1.3.1 Using the Electrical Parts List

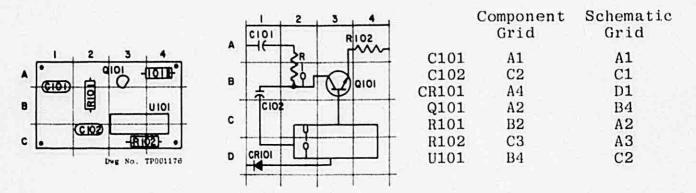
The action column identifies added, changed, and deleted parts, the effectivity column identifies the Chassis Level Configuration Code Letter used to identify when the part was effected.

To the far right of the part number/description one will find a grid coordinate listing for that part, one set of coordinates locates that part on the component assembly drawing, the second locates the part within the schematic. Where a part, such as an IC, is broken down into several subcomponents, each component part is located for the user.

6.1.3.1 Continued

Grid coordinates are shown on both the component assembly drawing and the schematic. The grids are not, in themselves, shown to avoid clutter.

The grid coordinate identifies that grid box where in the components symbol letter is located as shown in the sample below.



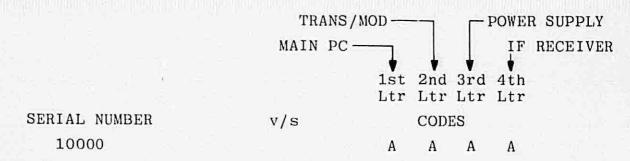
6.2 MODIFICATION LABEL

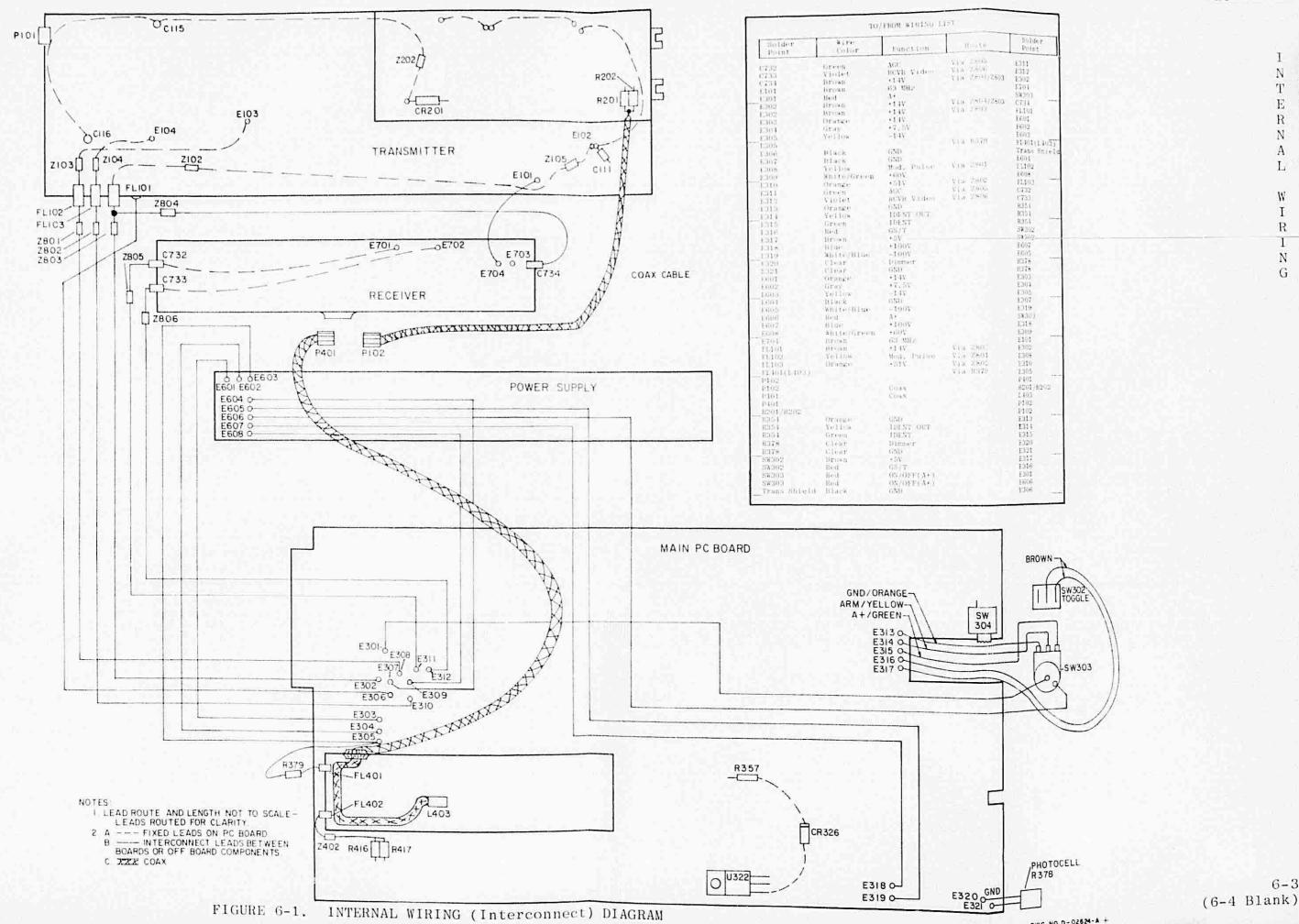
The modification label affixed to the unit is provided to allow quick recognition of what modifications where made to that unit, if any. Thus the block should only be filled in upon completion of a Narco Service Bulletin Modification Instruction. Fill in only that block or blocks that the Bulletin designates.

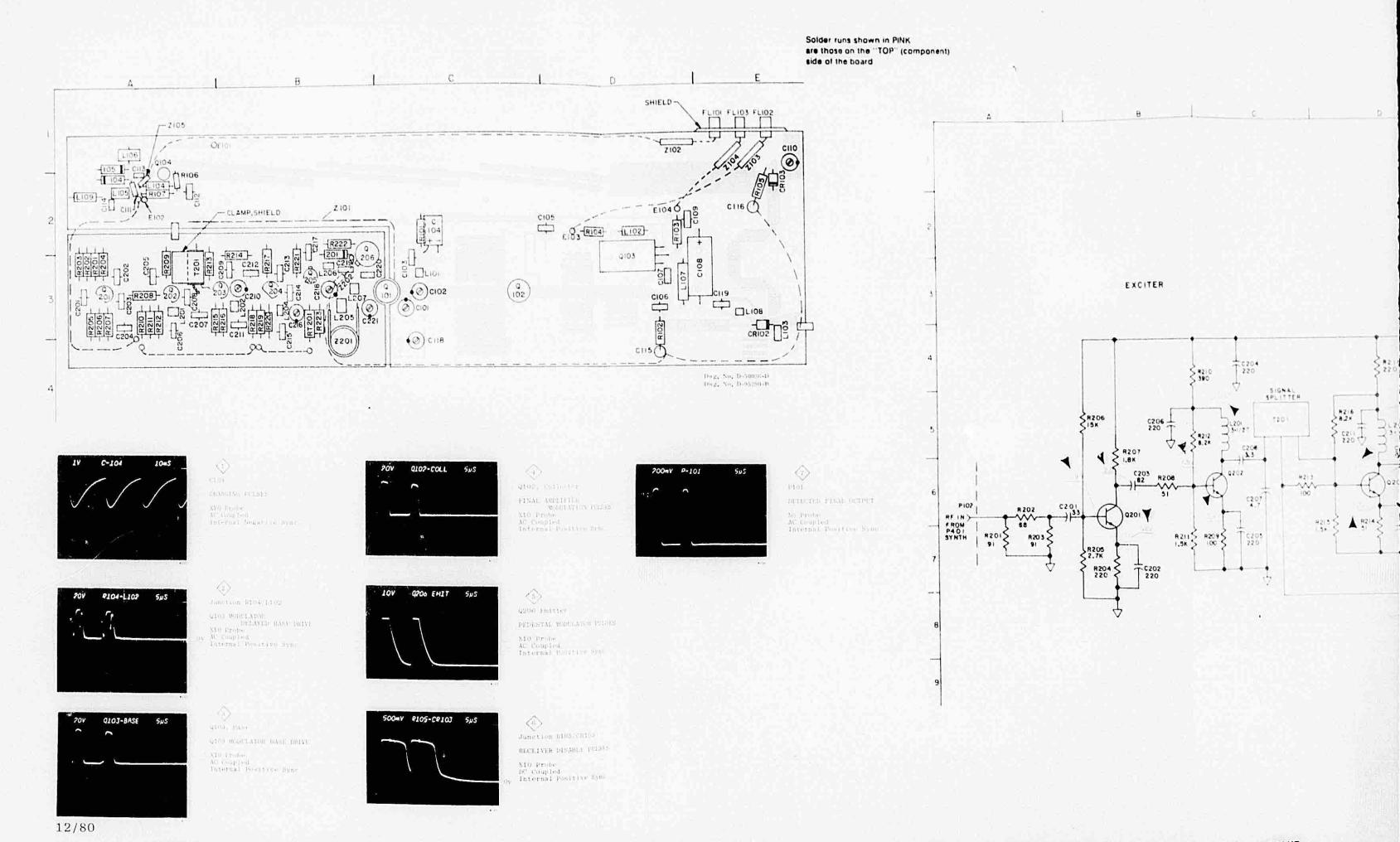
6.3 SERIAL NUMBER V/S CHASSIS LEVEL CONFIGURATION CODE

The Serial Number will be the key factor to identify units. The Chassis Level Configuration Codes will be used when necessary to identify specific subassemblies at specific levels.

When a Unit's Chassis Code is presented as a series of letters, their arrangement reflects:







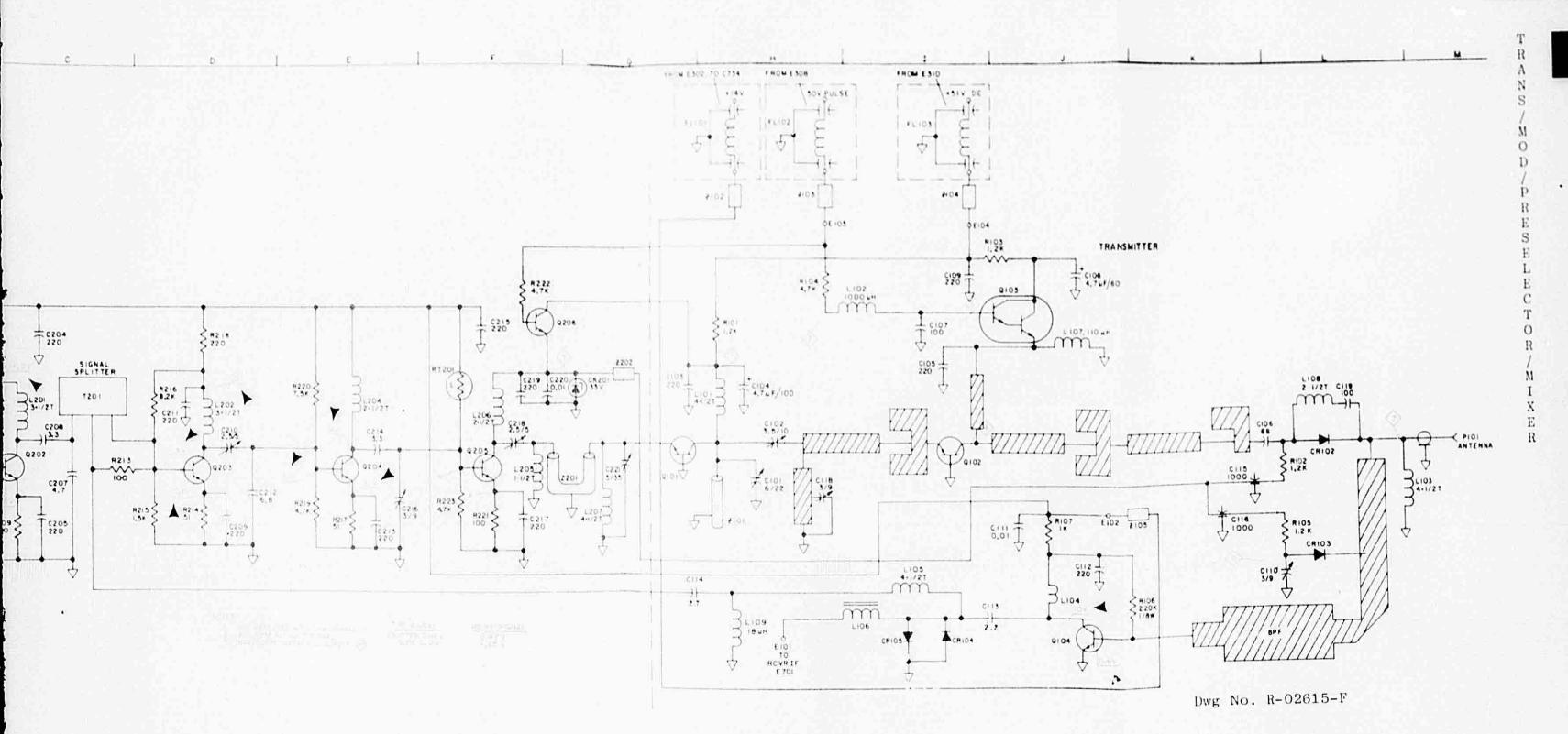


FIGURE 6-2. TRANS/MOD/PRESELECTOR/MIXER

DME: 890

FLECTRICAL PARTS 1487 LIST NO. 01376+01013

10	BASSA	LENGT CODE	ided, glanged, deleted.	Carl Cont	matks	N'S
	Symina	l. Number		Concessed A	128	1
		Part Number	Description			1
1.1					-1-	_t
		SECTION AND A	CAPACITOR			
o A	C102	22053-0003	Trimmer, d-32 pr. 1000 Ceramic, Trimmer, 3,5-10 presente, Transcrott, 220 pt	1 637	5.3	H4
0 8	0.102	24562-0024	France, Trapezoid, 220 pl	100 CV	123	64
i G			Electrolitic, 4.7 of *75. Ceramic, Trapezoid, 220 p)		10	13
u ş	C100	24562-0016	Ceramic, Trapezoid, espy	\$201, 831	00	K4
1 A	(108	21555-0170	Tantalum, 4.7 ur ton no	2003	03	13
1.8	(1)00	3456240021	Coramic, Mono, 100 pr 200 Tantalum, 4.7 ur -101, 600 Coramic, Traperoid, 200 pt	Leot. 63V	.02	15
×	3.3.471	A 8-1-13-1-100-1	A STATE OF STATE AND STATE AND STATE OF		EL	1,G
0 A	C112	24550-1408	Ceramic, Mono, .oi ni leon Ceramic, Transport, 200 at	1991	12	245
o A	2310	21552-1220	Ceramic, Trapezeid, 220 pl Ceramic, 2.2 pr 1.5 pl, 50 Ceramic, 2.7 pf5 pl, 50	W 1997	All	17
0 8 0 A	C115	21200-0008	Ceramic, 2.7 pF - 5 pF, 50 Ceramic, Feedthru, 1000 pp	N STO	A2	116
1 A			Coramic, Feedthru, 1000 pi			111
	1115	24563-0002	Trismer, 3-9 pF, 100V	201, 2300	e 1.	
0 A	6118	24005-0020	Ceramic, Trapezoid, 100 pl	F FIRE BOY	¥.th	1.4
			D1000			
0 1	CH102	75044-0001	Silicon, Switching, Pin		13	
XI. A	CHIDS	73071-0001	Silicon, Switching, Pin Microwave-Schottky ND4981	75	12	
0 8	CE1-05	75063-0001	Microwave-Schottky SD4981	-71	A1	
			FILTER			
		24564-0001			5.1	
		24564-0001 24564-0001			11	11
			CHOKE			
o A	1101	11713-0015	RF 4-1/2 Turns, .080 Dia.	Ttys :	(3)	H 4
0 A 2 A	1.103	11713-0015	1000 uF -10% PF 4-1/2 Turns, .080 Dis.	p.s.	1/3	ME ME
o A	1,104	00019-0022	RF Inductor #22 RF 4-1/2 Turns, 1080 Dia.		12	17
	L106	11935-0001	Toroid, & Turns, 1080 His. 110 uH, -54		A.1	17
n A	Dios	11713-0020	RF. 2-1/2 Turns 080 Dia	. P.S.	113	1.4
o A	£109	11451-0022	RF. 18 uH		A2	He
o A	P101 P102	41318-0001 41344-0001	CONNECTOR, PLUG CONNECTOR, PLUG			
			TRANS1STOR			
o: A	9101	75681-0001	RF, Microwave SSM SD 1528	-2/MSC80808	C3	G
(4) A:	Q163	75635-0007	RF, Microwave SSM SD1530- Silicon, Darlington, NPN	er ale subult	0.3	J:
o: A	0104	75679-0001	Microwave, NEC 73437		A1	J
. 2	10.1-		RESISTOR			
0: A: 0: A:	B102	31218-0122 31218-0122	Carbon, Film, 1.2K 75%, 1 Carbon, Film, 1.2K 75%, 1	\4M	C2 D4	H.
A A	10.10.03	31218-0122	Carbon, Film, 1.2K -5%, 1	/ 410	D3	1
a A	45.400.00	13 A to 1 C - 11 L C -	Carbon, Film, 4.7K 75%, 1 Carbon, Film, 1.2K 75%, 1	7.34.99	101	H L
o A	R106	31216-0224	Carbon, Film, 220K, -5%, 1 Carbon, Film, 1 K -5%, 1/	184	A2 A2	K J
or. A	2101	90119-0005	Coax, Formed Assy			Н
A 0	2102	11454-0009	Ferrite Bead Ferrite Bead		E1 E1	H
o A	2104	11454-0009	Ferrite Bead		E.1	1
o A	2105	11454-0009	Ferrite Bead		A2	J

DME 890 LIECTRICAL PARTS LIST LIST NO. 01381-01018

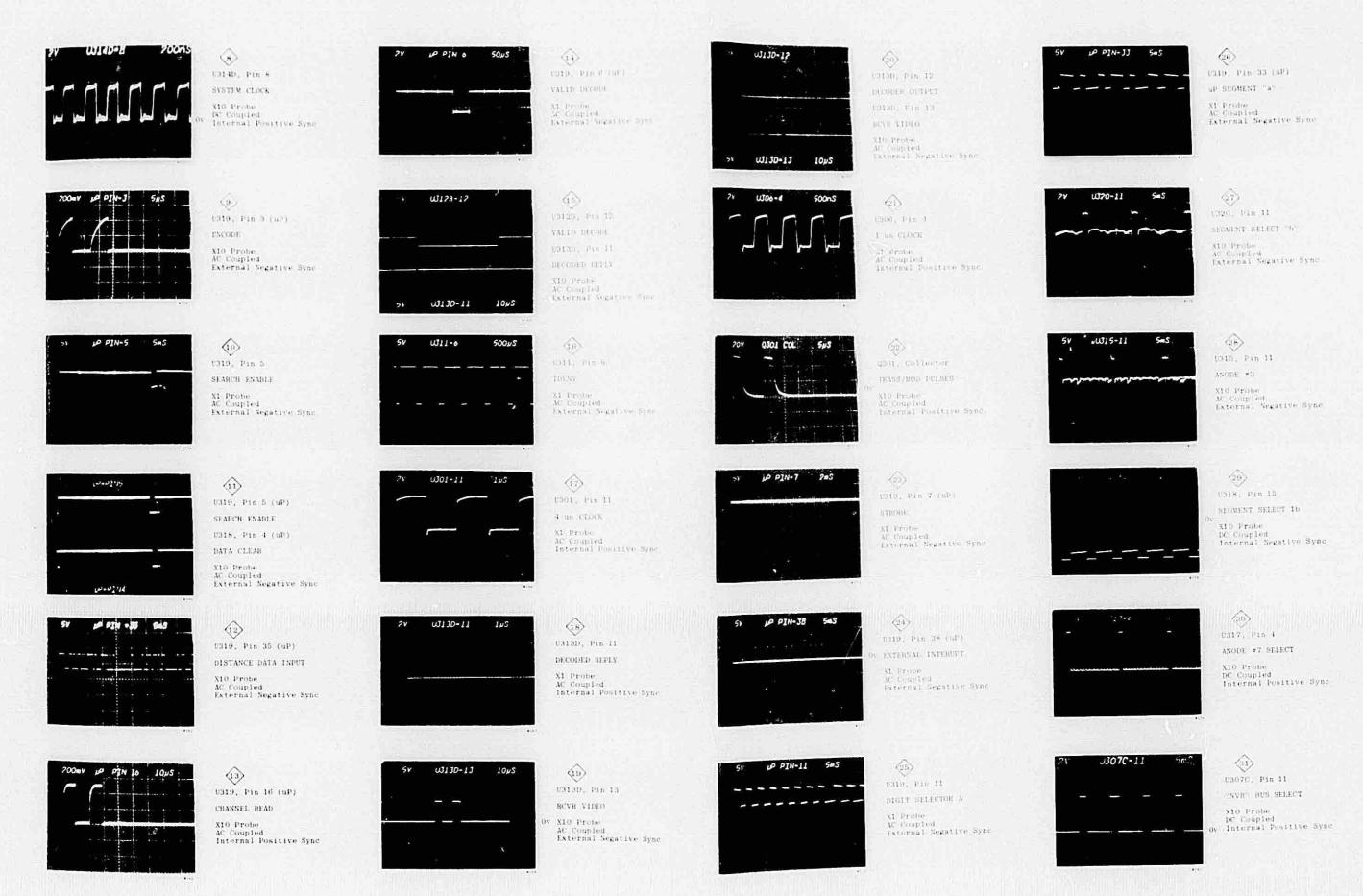
	base la	grigital, ad Level Code I Number	ded, ghanged, deleted. Grid Coord Schen- Component Av	110	
		Part Number	Description		,
			CAPACTTOR		
A	(min)	24562-0014	Coranic, Trapozold, 33 pF 191, 63V	A3 .	15
1 7		24502-0024		A1	
1 3	720353	24502-0010	Coramic Transported, 82 pt -107, 63V	43	13
i A	C201	24562-0024		31.	CX
- 3	2705	24502-0024	Ceramic, Trapezoid, 220 pf -20%, 63V	A3.	(1)
	emen	HARRIS DANK	Coramic, Trapezoid, 220 pf #20%, 63V	44	114
4	0.200	21502-1021			
1 4	20 miles	2 10112 1000	Ceramic, Trapezoid, 3.3 pt :0.5pf, 63V		04
3 1	27900	24502-0021	Ceramic, Trapezoid, 220 pf -207, 63V	83	50
A	C210	22053-0001		W3 =	
	CV13.3	market contra	Ceramic, Trapezoid, 220 pf -201, 634		ly s
a A	2793	94569-0004	Conserve Teampered 6.8 of -0.567.014		
a A	4793.5	9.15419 - 0091	Ceramic, Trapozoid, 220 pf 20%, 03V		136
o A	(91)	24562-0002	Ceramic, Trapezoid, 3.3 pt 10.5pt,63V		13
o A	0210	24562-0024	Ceramic, Trupozoid, 220 pt -201, 63V	BL.	13
	(2034)	2015371_0021	Tringer, 3-9 pF, 100V		
S A		24002-0024			
o A		22053-0001	Comment of Technology Of Such DF	11.9	
o a		24562-0024			10
CI A	(2000)	0.1550-0103	Ceramic, Mono, .01 uF -207, 100V		10
o A	622	24563-0005	Trumer, 5-35 PF, 100V	63.	
			рторг		
. X	CR201	75047-0005	Zener, 33V	112	
			co11.		
0.3	1.20	1.11713-0001	RF, 3-1/2 Turns080 Dis. P.S.	40	
0 1	1.200	2 11713-0004	RF, 3-1/2 Turns, .080 Dia, P.S.		D
57 d	1,20	1 11713-0020	RF, 2-1/2 Turns, .080 Din, P.S.	133	8
15 0	1.20	11713-0008	RF. 1-1/2 Turns125 Dia. P.S.	134	F
61.16	1.20	11713-0020	HF, 2-1/2 Turns, .080 Dia, P.S.	100	10
() i	1.30	7 11713-0015	RF, 4-1/2 Turns, .080 Dia. P.S.	NI	1.0
			THANSISTOR		
0. /	1 020	1 75677-0001	NEC 73432B	43	
10 6	4 Q20			14.3	15
0.1			NEC 73432B		P
0.7			NEC 41632B	11.1	
(3. J			SSM SD 1379-8	403	3
O 14	A 020	6 75536-0003	2N3053	DO:	1

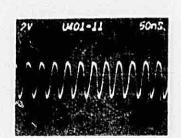
			Level Code Number	1			Schoma Component Ass		
			Part Number		1	escription		1	٠
					1	ESISTOR			
	λ.	RESIDE	31918-0910	Carton	Frim.	91 75%, 1/4%		9.90	A6
П	À	B202	31218-0680	Carbon	Film.	68 +5%, 1/4%	-	13	
	4	8209	31218-0910	Carbon	Film.	08 -5%, 1/4% 91 -5%, 1/4%		13	A6 B6
	3.	102004	20120190200221	Carbon	1 1 1 1 1 1 1 1 1	220 -04, 479		13	B6
6	Ä.	1205	31218-0272	Carbon	Film.	2,78 -5%, 1/	14	13	1345
	3	8206	31218-0153	Carbon	Film.	15K -5%, 1/4	K	13.	
	À	R207	31218-0182	Carbon	Film.	1.85 -5%, 1/	1 A	13	
	Ä	H208	31218-0510	Carbon	Film.	51 -5%, 1/4W		13	
	A .	11309	31218-0101	Carbon	Film,	1.86 -5% 1/ 51 -5% 1/4W 100 -5% 1/4	6	¥3:	
f	Λ	11310	31218-0391	Carbon	Film.	300 -5%, 1/4	А	A3:	C3
	Ä	11911	31218-0152	Carbon	Film.	1.58 -5%. 1/			B6
	Ä	8212	31218-0822	Carbon	Film,	8,28, -5%, 1/	18	13	
v.	Ä	R213	31218-0101	Carbon	Film.	8,28,-5%, 1/ 100,-5%, 1/3	K	2.77	(05)
	A.	14000 414	- Tel 22 1 N = D25 1 D	CAPDODI	1 1 1 1 1 1 1	D1 = D4 - 4 / 10			D5
λ	A	R215	31218-0152	Cartion	Film,	1.58 -5%, 1/	19	4-3	D5
	A	10216	31218-0822	Carbon	Film.	8,2,-5%, 1/4	w I		10.4
	A	8217	31218-0510	Carbon	Film.	51 -5%, 1/4W		83	E6
,	A	B218	31218-0221	Carbon	Film.	51 -51, 1/1W 220 -5%, 1/4	X.	193	D3
	ā.	E210	31218-0472	Carbon	Film,	7.5K -5%, 1/	4W	83 83	E5
gr)	A	R220	31218-0752	Carbon	Film,	7.58 -5%, 1/			
	4	8221	31218-0101	Carbon	Film,	100 -57, 1/4		83	F6
6	A	R222	31218-0472	Carbon	Film,	4.78 -5%, 1/	1W	H2	F5
0	A	R223	31218-0472	Carbon	Film,	1.7K ±5%, 1/ 1.7K ±5%, 1/	4W	15.3	1.0
						THERMISTOR			
				. 6000	home or			B3:	F.5
0	A	10.550	1 31214-022	2 2200 C	PERIOD.				
						TRANSFORMER			
		200	1 11934-000	1 Halun				A3	C
1	14	140	* ********						
1	i	993	1 90119-000	7 COAX	Former	1 Assembly		84	-
10	1	7.20	2 11454-000	9 Ferri	te Bear	1		B2	GE
1	7.5								

C304

C305 C306 C307 C308

€ 309





OHI, Birds

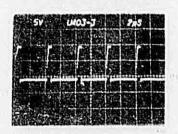
JOH, Birds

JOH, Birds

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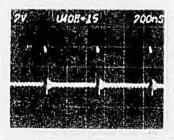


CONTRACTORS

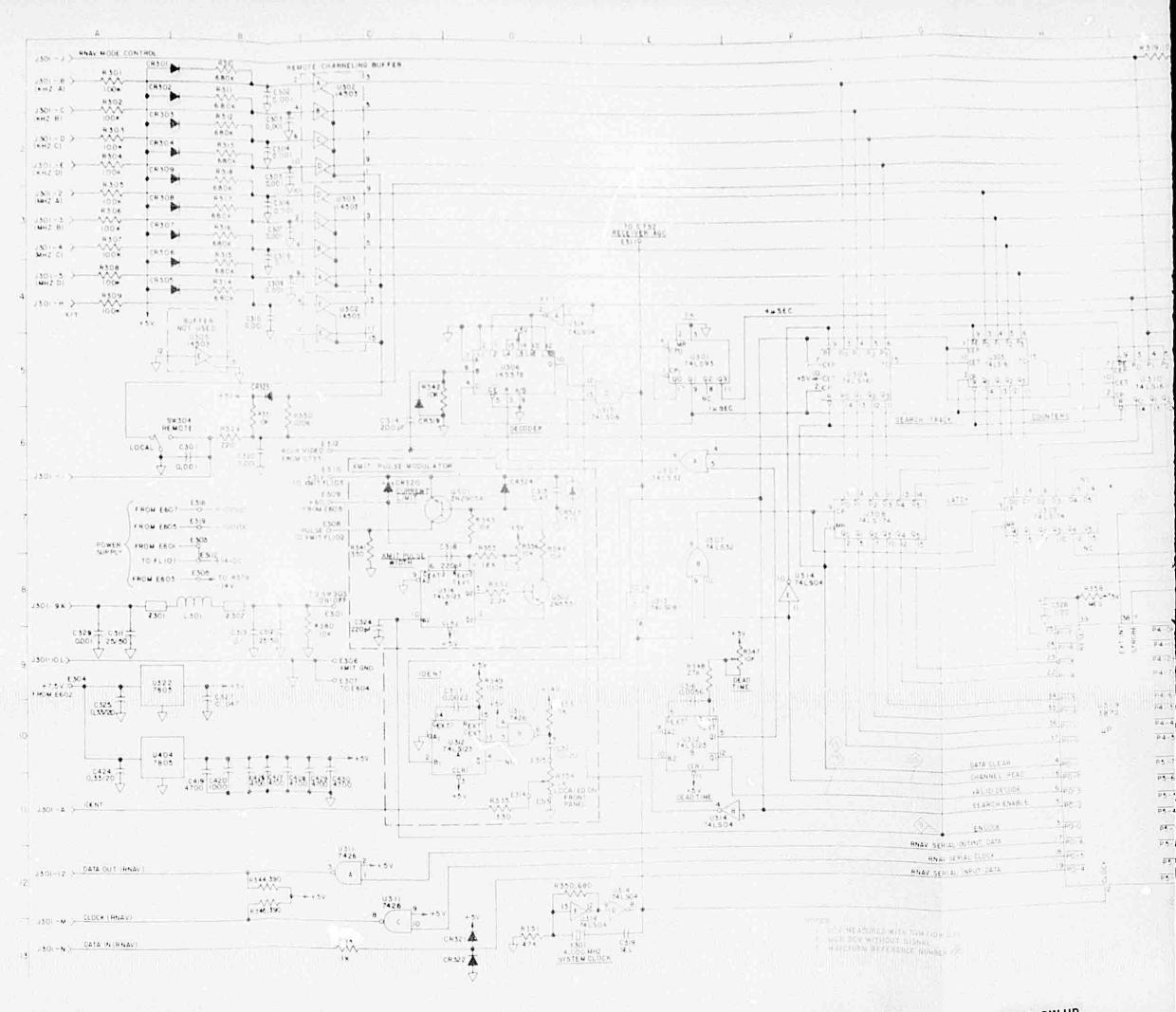
STORETH COTORS

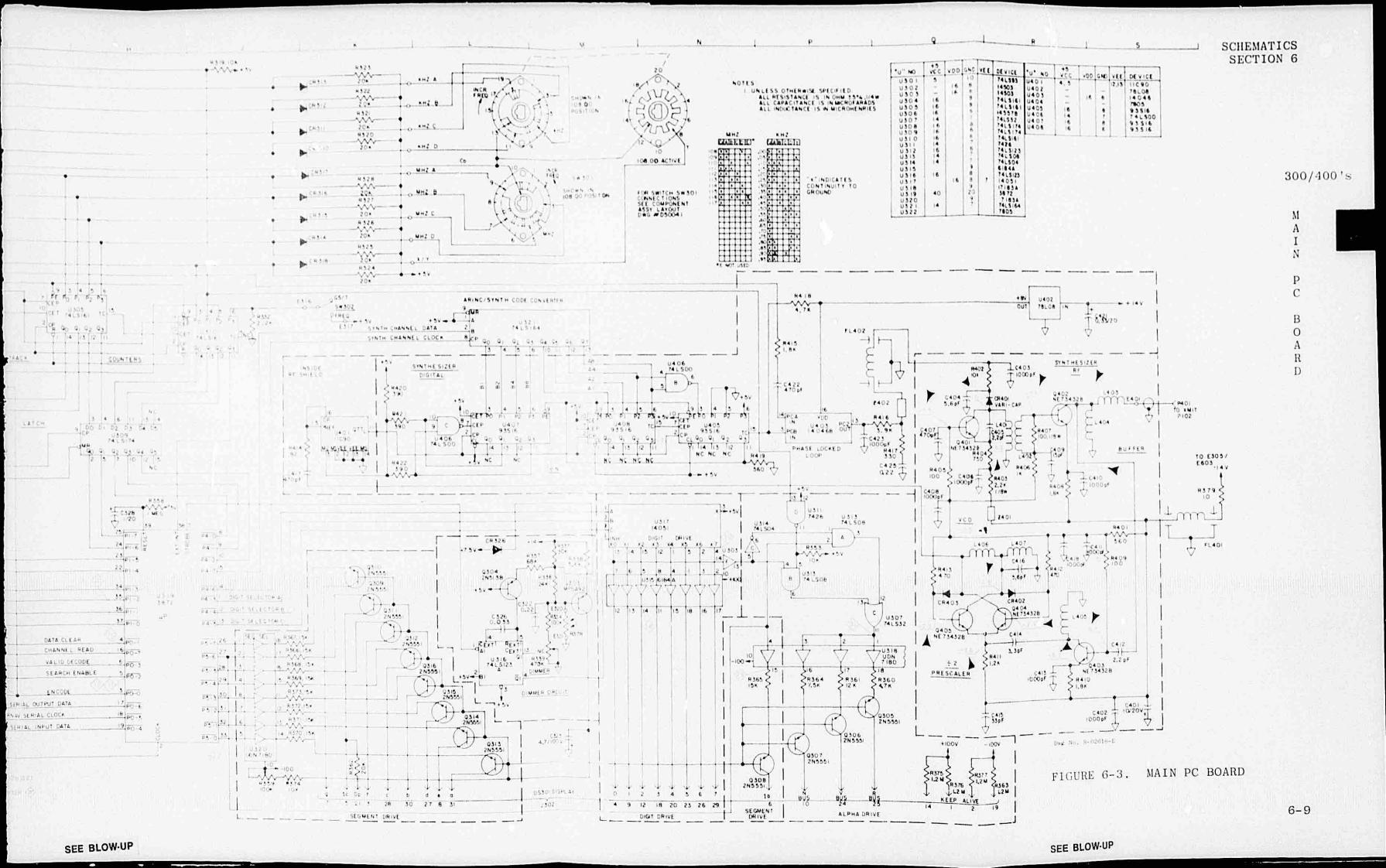
After the system

A



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6-10

ELECT	RICA	d. PARTS 1.187
LIST	50;	01378-01013
g to	hange	d, deleted.

Ver I	on: original, ad	ded, changed, deleted,	Grid Coord	imit da
(Cb)	issis level Code. Symbol Number		Schem Component As	ALL LOSS
	Part Number	beseruption		
1 1		CAPACT TOR		
o A o A o A o A	C302 24551-0005 C303 24551-0005 C304 24551-0005 C305 24551-0005	Ceramic, 1000 pF -10%, Ceramic, 1000 pF -10%, Ceramic, 1000 pF -10%, Ceramic, 1000 pF -10%,	100V 100V 100V 100V	A2 B6 A2 B1 B1 B2 B1 B2 B4 B2
0 A 0 A 0 A 0 A	C307 24551-0005 C308 24551-0005 C309 24551-0005 C310 24551-0005	Coramic 1000 pf 10%, Coramic 1000 pf 10%, Coramic 1000 pf 10%, Coramic 1000 pf 10%, Coramic 1000 pf 10%,	100V 100V 100V	61 93 51 63 51 63 51 10 73 114
A 0 A C A C A C A C A C A C A C A C A C	C312 21554-0006 C313 24550-0104 C314 24052-0201 C315 23113-0103	Floatrulytte, 25 mF +10 Floatrulytte, 25 mF +10 Ceramic Mone, 0.1 mF -1 Micu, 200 pF -5%, 300V Mctal Poly, 0.47 mF -10	0% - 150%, 50V 20%, 100V	A4 148 A4 148 101 148 101 106 104 167
0 A 0 A 0 A 0 A	CHS 24052-0221	Poly Film, .0056 mF 55 Poly Film, .0022 mF -5 Mica, 220 pF -57, 300V Wica, SPL -57, 300V Ceramic, .001 mF -104.		01 19 01 09 14 07 14 07 15 06
0. A 0 A 0 A 0 A	0322 23113-0101 0323 21507-0024 0324 24052-0221 0325 21508-1074	Tantalum, 10 mF -20%, Motal Poly, 0.22 mF -1 Flectrolytic, 4.7 mF Mica, 220 pF -57, 2008 Tantalum, 0.33 mF -20%	07, 100V 75% -10H, 100V -20V	11 010 14 010 11 912 05 Cs 07 410
6 A 6 A 6 A	CH28 21508-10473	Poly Film, $33~\mathrm{mF}-5\%$. German, Mono, $1047~\mathrm{mF}$ lantalum, 1 mF -20% . 2 German, $001~\mathrm{mF}-10\%$	OV	DO 1.10- DO 100 DO 108 A3 A9
		CAPACITOR		
o A	C401 21568-1092 C402 24562-0032	Tantalum, 10 mF 20%, Ceramic, Trapezoid,	20V -209, 63V	A30 542
0:3	(40) 24562-0032	AND THE RESERVE OF THE PARTY OF		
0 A	C404 24552-150/ C406 24552-1229	Ceramic, Trapezoia 1000 pf +807 Ceramic, 5.6 pF +.5 pf Ceramic, 2.2 pF5 pf	NPO 50V	A. 196
.o. A	C406 24562+0033	Ceramic Trapezoid. 1000 pt 1802 - Ceramic 170 pt -205.	-205 63V	36 US 40 07
0 1	C108_21542+0033	toranio, trapezota 1000 of •800	-20%, 63V	16 08
0 A	C109 24552-1156 C110 24502-0031	Ceramic, Trapezoid, 1: Ceramic, Trapezoid, 1000 pF *80	5 pF =10%, 50V -20%, 63V	B5 178
D. 1	C411 24562±003	Ceramic Trapezoid 1000 pF (80%	-20% 69V	161 161
2.7	0412 24552-122) Coramic, Trapezold, 2.2 pF5 p		116 811
10.1		1000 pF +80%	-20%, 63V F 50V NPO	8d 111
0	0415 24552=133	9 Ceramic, 3.3 pF - 5 p 9 Ceramic, 33 pF - 5 p	Fig. 2004 Care	D6 R13
Q1	\ 0410 24552-156 \ 0417 24551-000 \ 0418 24562-003	9 Ceramic, 5.6 pF + 5 p 2 Ceramic, 170 pF + 20%, 2 Ceramic, Trapezoid,		H5 H8
0	A C419 24550-047 A C420 24562-003	9 Covers Transcould	G., 100V	C5 R9
10	A 0422 24551-000 A 0423 24551-000 A 0424 24568-107	1000 pt *805 4 Tantalum, 0.33 mt -20 2 Ceramic, 470 pf -20 4 Ceramic, 1000 pf -10 4 Ceramic, Tantalum, 0 1 Metal Poly, 0.22 mf	05 20V 50V 100V 33 mF = 205 20V	A6 07 A6 07 A6 07 A6 17 106 A1 108 07

		original, added, Level Code	manged, defeted;	Grid Coor Schi	mot Lie	
		a Number		Component		
		Dart Number	Description			1
1_1			CAPACITOR			
1 A 10 A 10 A 10 A 10 A 11 A 11 A	C42 C42	7 24550-0472 Ceru 8 21550-0472 Ceru 9 24550-0472 Ceru	mic, Mana, 10047 mF	20% 100V 20% 100V	B7 B6 C6	111 111 111 111
			DIODE			- [
6 A	CH30 CH30 CH30 CH30 CH30	2 75028-0001 S111 3 75028-0001 S111 4 75028-0001 S111	eon, Switching, 25V con, Switching, 25V con, Switching, 25V		A3 A3	A1 A1 A2 A2 A3
0.7	CHECK CHECK	6 75028-0001 S111 17 75028-0001 S111 18 75028-0001 S111 19 75028-0001 S111 0 75028-0001 S111	con Switching, 25V con Switching, 25V con, Switching, 25V			A3 A3 A2 A2 82
	A CHS	2 75028-0001 \$113 13 75028-0001 \$113 14 75028-0001 \$113	con Switching, 250 con Switching, 250		02 02 02 02 02	K2 K1 K1 K1 K1 K1
17	A CRS. A CRS. A CRS. A CRS. A CRS.	17 75028-0001 Sili 18 75028-0001 Sili 19 75028-0001 Sili			132 132 132 133 134	K3 K4 C6 C7
3 2 2 2	A CRIA A CRIA A CRIA A CRIA A CRIA A CRIA	22 75028-0001 Sti 23 75047-0007 Zens 24 75028-0001 Sti 25 75028-0001 Sti	icon, Switching, 25t er. 54V, 75 icon, Switching, 25t roon, Switching, 25t		11 4 13 4 10 4 13 4 13 6 13 6	013 07 07 07 09 10
			nton			
1	A 1786	61 73043-0601 S12 62 75028-0001 S12 63 75028-0001 S11	reon. Switching, 25		A5; B5 B5	116 Q10
			DESPLAY			
-17	A DS	01 50014-0001 018	PLAY, Gas Discherge		15	MI
0	A di	502 50231-0001 CON	Connector EXECTOR, Display			
			FILTER			
		101 24564-0001 EMI 102 24564-0001 EMI			44 45	TP P5
10	Ä i	301 11 (87-0002 Fi	rter		.A3	B8
			CHOKE			
0 0 0 0	A L A L A L A L	403 11713-0015 RF 404 11713-0005 RF 405 11713-0004 RF	P.S. 1-1/2 Turns P.S. 1-1/2 Turns P.S. 7-1/2 Turns P.S. 3-1/2 Turns P.S. 3-1/2 Turns		85 85 85 85 85	87 87 80 87 81 99
1			CONNECTOR			

o A P401 41244-0002 Connector, Jack

	117	come I	riginal, ad level Code Sumber	ded, <u>c</u> ha	uged.	deleted,		- Grid Cos Sci Component	nemntic	
	,		Part Sumber		De	scriptio	n			
					71	(ANSISTO)				
	À	Q102 Q103 Q104	73634-0001 73070-0001 73070-0002 73506-0001 73075-0001	Silteon. Silteon. Silteon.	PNP, PNP,	2N5551. MPSA02, 2N5138	200V		E4 E4 D5 E4	D7 D8 M10 L9 Q12
	1000	0303 0303 0307	75075-0001 75075-0001 75075-0001 75075-0001 75075-0001	Silicon Silicon Silicon Silicon	NPN, NPN, NPN, NPN,	2N5551, 2N5551, 2N5551,	140V 140V 140V 140V		E4 E5 E5 E5 E5	P12 P12 N13 K9 E9
	4	0012 0317 0017	75070-0001 75075-0001 75075-0001 75075-0001 75075-0001 75075-0001	Silicon Silicon Silicon Ellicon	NPN.	285551, 285551, 285551, 285551,	140V 140V 140V		E5 E6 E6 E6 E6	K10 K10 L11 L12 L12 L12
	A.	Q 102 Q 103 D 103	75677-0001 75677-0001 75677-0001 75677-0001 75677-0001	Microso Microso	se Ni se Ni	N. NEC73 N. NEC73 N. NEC73	432B 432B		A5 B5 B5 B5 B5	Q7 R6 R11 R10 Q10
					î	d.stston				
	LANA	#11/1/2 - #11/1/2 - #14/0/3	31218-0104 31218-0104 31218-0104 31218-0104 31218-0104	Carbon Carbon Laphon	Falm. Falm.	100K -51 100K -51 100K -51		136 136	A2 A2 A2 A2 A2	A1 A1 A2 A2 A2 A2
0.28	1 A A	11303 11308	11218-0101 11218-0101 11218-0101 11118-0101	Carton	Film.	100K -00		196 196 196	A2 A2 A3 A3 A3	A3 A3 A4 A4 B1
	1 1	TOR	11018-008 11018-068 11018-068 11018-068 11018-068	Carlon Carbon Carbon	Film:	080K -00	1	IW IW	A2 A2 A2 B3 B3	B2 H2
		Pata Pata Haar	1 11218-068 31218-068 31218-068 31218-010 31218-010	Carbon Carbon Carbon Carbon		680K -5' 680K -5' 40K -5'	1/ 1/ 1/ 1/	IW IW IW W	83 83 83 83 62	B3 B2 J1
		1 832 1 832 1 832 1 832	1 31218-020 2 31248-020 3 31218-020 4 31218-020 5 11218-020	S Carbon B Carbon B Carbon	F : 1m : F : 1m : F : 1m :	20K -59 20K -59 20K -59 20K -59	1/d 1/d 1/d	II. A. II.	C2 C2 C2 C1	K1 K1 K1
	0	A RM2 A RM2 A RM2 A RM2	0 31218-020 7 31218-020 8 31218-020 9 31218-022 0 31218-010	i thelen i Carbos i Carbos	Film Film Film Film	20K +5% 20K +5% 20K +5% 220 -5%	1/- 1/- 1/- 1/-	W.	C2 D2 D2 E3	E3 K3 B6
		A Rail A 1983 A 1983 A 1983	1 01218-010 ĝ 31218-022 3 31218-010 4 31218-010 5 31218-03	G Carbon 2 Carbon 2 Carbon	Film Film Film	106 - 51 2.26 - 5 16 - 51 1006 - 5	1 /- 1 / 1 1 / 1	1% - ‡% 1 1 1%	E: E: E: E:	1 J5 3 D10 3 M10
	0.000	A HOU A HOU A HOU A HOU	66 31218-02 67 31218-036 68 31218-036 69 32054-00 60 32054-00	D Carbo B Carbo B Carbo	n Film H Film n Film	24K ±57 30K =57 5.0K =170K (Dim	1. 1/ 1. 1/ 51. 1	1 W 2 M 3 M	† † †	3 M9 3 M9 2 L1

Actio	n. or	1231	161.	ada	lett.
S	Ampol .	Num	regr :	(te	
	į.	art	None	her:	
	R041 0 R041 0 R041 0	121 121 121	8+01 8+01 8+0)	03 03 91	Carb Carb Carb Carb
6 A 6 A 6 A 9 A	#317 3 #348 3 #348 3	207 121 121	5×01	104 175 104	Carb Vari Cart Cart Cart
0 A 0 A 0 A 0 A	R352 A R353 I R354 J	3121 3121 3201	(8=0 (0=0	992 103 003	
6 0 4 0 4 0 4 0 8 0	R057 R058 R050	312 312 320	(6-0 18-0 18-0 18-0	683 105 1012	Var
0. A 0 A 0 A 0 A 0 A	1000 1000 1004	312 312 612		1200 120 1732	Car
0 A 0 A 0 A 0 A 0 A	H266 H267 H268 R269 R370	312 312 312	18-0 18-0 18-0 18-0	01.50 01.50 03.50	Car Car
0 A 0 A 0 A 1 A	1071 R372 R373 R374 R376	33.2 33.4 33.1	18- 18- 18- 18-	015; 016; 016;	Can Can Can
o A o A o A o A o A		312 312 311 312	115-	022 000 010 010	Pho Ca Ca Ca
o A o A o A o A	R403	312 312 312	218- 216- 218- 218-	010 022 075 010	
0 A 0 A 0 A 0 A 0 A	R-106 R-107 R-108 R-109 R-110	313	218- 218- 218-	010 018 010	1 Ca 1 Ca 2 Ca 1 Ca 1 Ca
0 A 0 A 0 A 0 A 0 A	R413	31:	218- 218- 218- 218- 218-	047 047 082	1 Ca 1 Ca 0 Ca
O A O A O A O A	R419 R420 R421	31: 31: 31: 31: 31:	218- 218- 218- 218-	037 047 056 039	1 Ca 2 Ca 1 Ca 1 Ca 1 Ca
0 A 0 A 0 A	SW301 SW362 SW303 SW304	61	358- 497-	-000	7 T€

Action: original, added, changed, deleted.
| Chassis Level Code
| Symbol Number

O A R341 31218-0331 Carbon Film, 330 \$58. 1/4W O A R342 31218-0103 Carbon Film, 108 \$55. 1/4W O A R343 31218-0103 Carbon Film, 108 \$55. 1/4W O A R343 31218-0391 Carbon Film, 390 \$55. 1/4W O A R345 31218-0391 Carbon Film, 390 \$55. 1/4W

Part Number

nerdinates nerativ

1 1

81 D7 C1 D8 E4 W10 D5 L0 T4 Q12

11.0	114	55.15	riginal, ad Lovel Code Number	ded chammed, deleted. Grid Coer Sche Component A	matti	
, ,	,		Page Number	Description	1	•
				10		
6 A	V	noi	74048-0002	4 (Gri Binary Cate 74LS93 (LST ² L)	B3 C2	E5
o A o A	U 0	302 3024 3024 3026 3020	74213-0001	Hex Traestate Potter 14503 (CMOS)		C1 C1 C2
		3020				02 01
0 4	1	302F 303 303A	74213-0001	Hex Tri-State Butter 14503 (CMOS)	C3	C4
0: A	i U	303B 303C 303D 303E 303E				C3 C3 C3 B4 N9
D A	. 1	304	74043-0302	Synchronous 4 Hit Binary Cutr		
0 A	1	305		74LS161 (LST*L) Synchronous + Bir Himmry Cutr		F5
0.7	v t	900		74LS181 (LST ² L) 1/64 Bit Variable Length 578	D3	G5
				- 14557b. (CMOS)	83	Db
3	1 1	307 307A 307B 307C		Quoid 2 luput OR Gate 74LS32 (LST ² L)	(73	E7 E8 Q10
		308	74176-0001	$\text{Rex} \text{ D-FT1} \text{p-FT0} \text{p-T4LS174 (18T}_{2}^{2}\text{L)}$	C3	67
		309 310		Box 1/Flip-Flop 74LS174 (LST*L) Synchronous 4 Lit Binary Cutr	93	H7
0 /	1 1	311	74234-0001	7418161 (LST*1.) Quad 2 input NAND Gate Wi Volt,	D3	UD
		311A 311D		7426TT4.	B4	C12 D10
		311C				C11
13.3	1	514 1D 1312		Dual S.S. Walt: 7415123 (LST ² L)	C4	P8
		3312A 3312B				D10 E10
0.0		E313 E313A	74024-0002	Quad 2 Input AND Gate $74 \text{LSO8} (\text{LST}^2 \text{L})$	C4	p9
0 :		J313B J313C				P9 E8
0.,	A 1	J313D				E5
0 1		1314 1314A	74051-0003	Hex Inverter 74LSO4 (LST ² L)	D4	D4
		J314B J314C				E1 N8
		0314D 0314E				E4:
		U314F				F8 D1
O.	A 1	U315 U315A UU15B		Octal Hivoltage Digit Driver UDN6184A	E4	:N9
0. 0.	A I	U316 U316A U316B	74062-0002	Dual S.S. Multi 74LS123 (LST ² L)	D5	CS L1
o.	A	U317	7-11-23-0001	8 But Multiples/Dimultiples 14051		
0.	A A A	U318 U319 U320 U321 U322	74215-0001 74214-0001 74215-0001 74170-0001	(CMOS) Octal Hivoltage Seg. Driver UDN7180A Microprocessor, 3872 Octal Hivoltage Digit Driver UDN7180A 1N/P. OUR Shift Reg., 74LS164 (LST-L) 5V Regulator, -2% 1 Amp, 7805	D5 E5 D6 E6 C6	N8 Q1 H1 J1 L5 A9

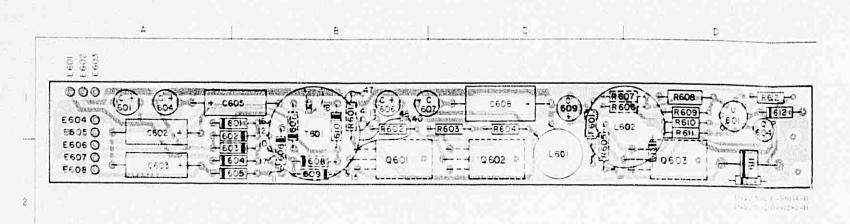
	Chassis Level Code Schema Component Ass						
1	•	,	Part Number	Description		,	
		U401	74068-0003	UHF High Speed Prescaler, 11090	C5	К7	
				8V Reg., 10-mA, 78L08	A6	R5	
		0.403	74119-0001	Phase Locked Loop, 40-16B (CMOS)	AG	P7	
		1404	74039-0002	5V Regulator, 243 1 Amp, 7805 Synchronous, 4 Bit Binary Chtr	13.6	A10	
		D-1011	1 (2111-0111)	93S16 (ST ² L)	B6.	N7	
(X	Λ	11406	74019-0002	Quad. 2 Input NAND Gate 74LS00 (LST2L)	13.7		
Ù.	A	U-106A					
ij	A	C4068				N6	
O.	A	P406C				1.7	
O	A	U407	74218-0001	Synchronous ₂ 4 Bit Binary Cntr 93816 (ST ² L)	CG	1.7	
15	A	0408	74218-0001	Synchronous, 4 Bit Binary Cntr	-		
		0.7420	A.14 1.01910.1	93S16 (ST ² i.)	C7	M7	
				CRYSTAL.			
Ó	.A	Y301	72064-0901	Quartz, 4.000 MHz	D4	D1:	
				BEADS			
o.	A	2301	11454-0003	Ferrite Bead	A3	A8	
Ü	a	2302	11454-0003	Ferrite Bead	B3	138	
13	A	2401	11454-0003	Ferrite Bond	A5	58	
				Ferrite Bead	AG	RG	

Grid Coordinates

Component Assy

Schematich

B3 | 07 03 | 05 04 | 17 B4 | B12 B4 | B13



Solder runs shown in GREY are those on the "BOTTOM" (non-component) side of the board.

Solder runs shown in PINK are those on the "TOP" (component) side of the board.



Secondary Second

DEGIT
SWITTHING FOLIAGE

KIN Probe
IC COMPLETE
IC COMPLETE
INTERNAL POSITIVE TYPE

2001. Vollenter
IRANSFORME SWITCHING VOLTAGE

110 Probe
Internal Positive Sync

FROM 3W303 0509 ±1 47/35V T 0604 2N2907A 2 U6 01 RE OB R610 , \$8607 9.09K 1% R612 2.7M 2.87 K \$ R601 R6115 7601 L602 3A TO E304 E602 0 +7.5 CR613 4,3V,5% +1 C608 206109 CR614 4.3V,5% 0602 2 N 6109 T C607 220/10V -- E6040 TO E 307 R\$02 NOTES:
I, UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IS IN OHM ±5%, 1/4W
ALL CAPACITANCE IS IN MICROFARADS DOV MEASUR DVM (10 m.O. 2 WOS DOV WI 3 WATEFORM H NUMBER

FIGUI

12/80

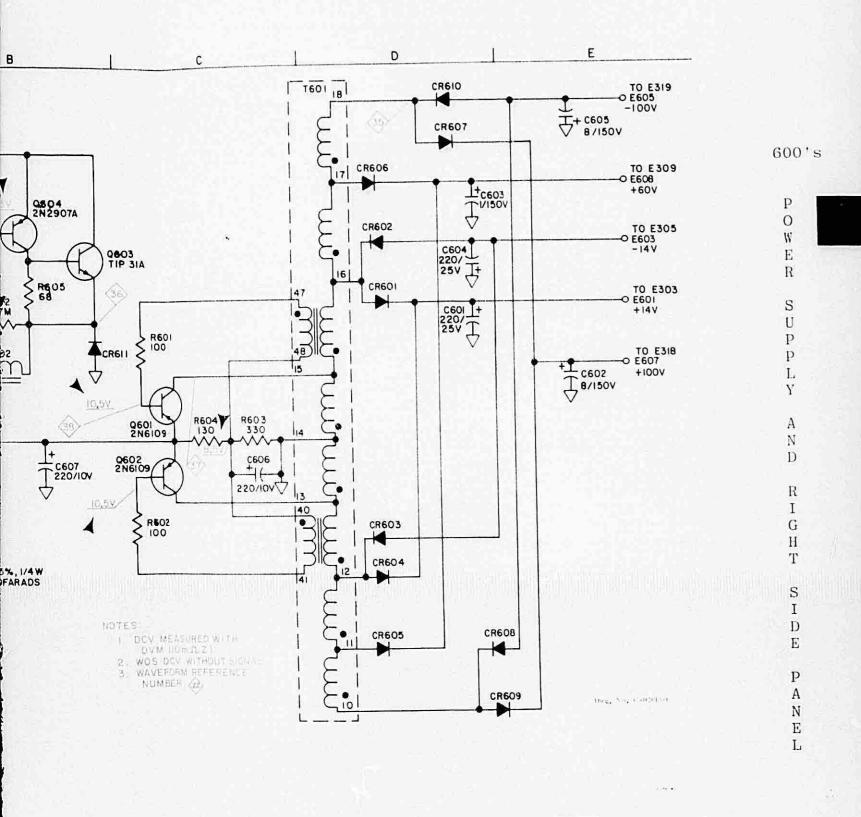
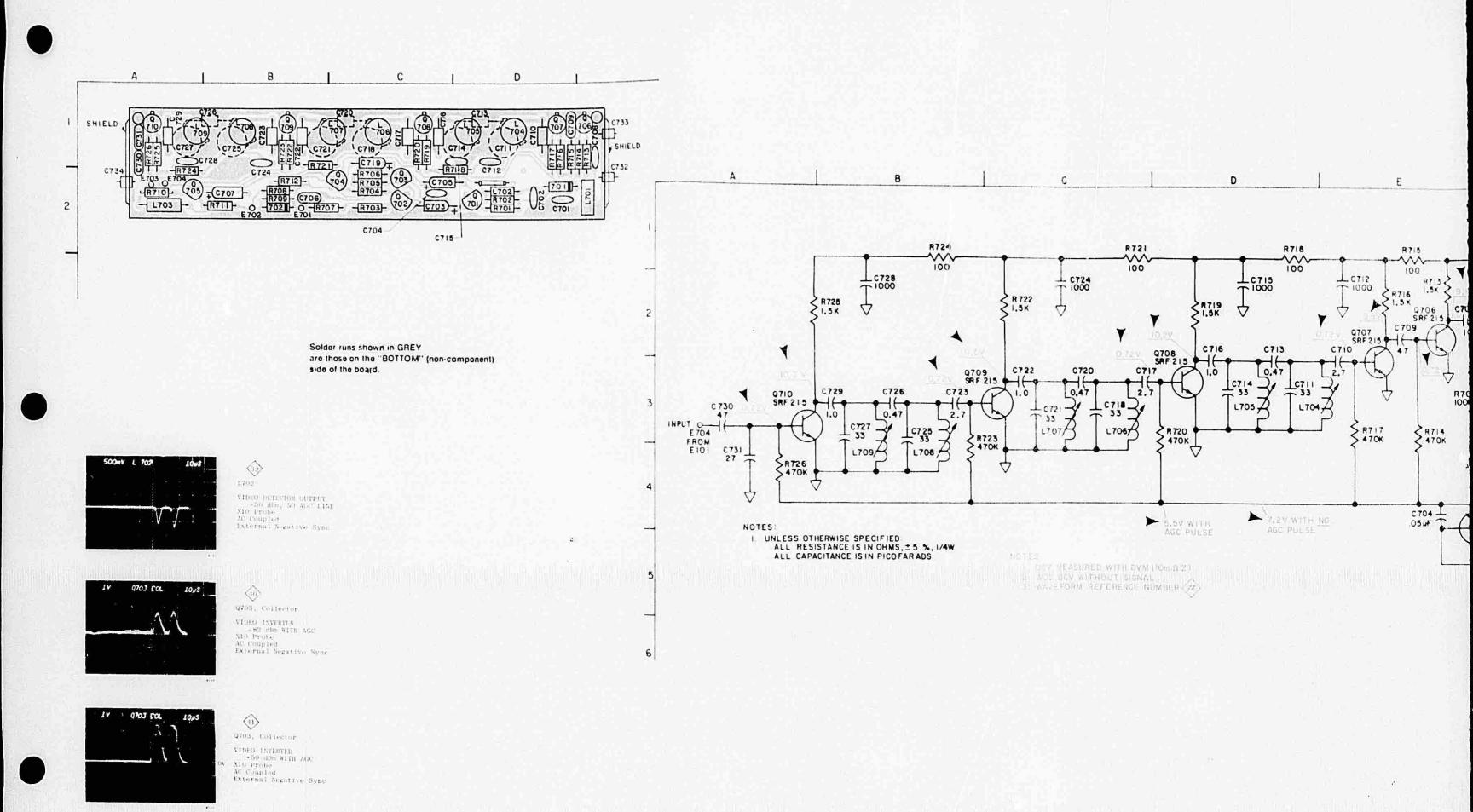


FIGURE 6-4. POWER SUPPLY AND RIGHT SIDE PANEL



12/80

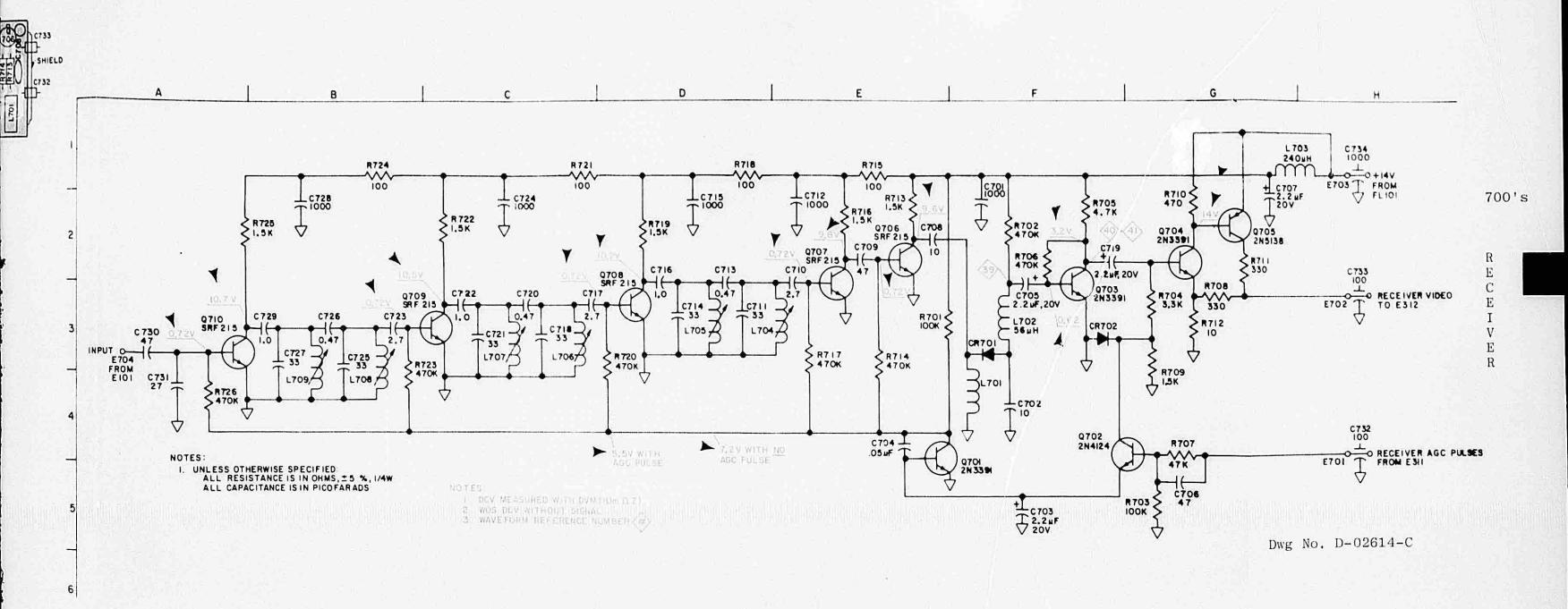


FIGURE 6-5 IF RECEIVER

DME 890 ELECTRICAL PARTS LIST LIST NO. 01375-01018

1.5	nassis	Priginal, ad Level Code Number	ded, ghangou, deleted. Grid Coo Sch Component	emat b	
		Part Number	Description		
Serie S			CAPACITOE		
0. A	C702 C703 C704	24516-0100 21568-1084 24515-0007	Coramic, 1000 pF -10%, 500V Coramic, 10 pF -1, pF, 500V Tanialum, 2:2 mF -20%, 20V Coramic, .05 mF +80T -20%, 20V Tanialum, 2:2 mF -20%, 20V		F1 F4 F5 E4 F3
0 A 0 A 0 A	C707 C708 C709	21568-1081 24516-0100 24052-0470	Miva. 17 pF -87. 300V Tantalum, 2.2 mF -207. 20V Cerumic. 10 pF -1pF, 500V NPO Mica. 47 pF -80. 300V Cerumic. 2 T pF -58. 500V	52 52 54 54 54	65 61 12 12 12 12
0 A 0 A 0 A 0 A	C712 C713 C714	21201-0019 24509-0478 24553-0001	Ceramic, 4.7 pF -20, 500V NPO Ceramic, 1000 pF -107, 500V Ceramic, 47 pF -57, 500V Ceramic, 93 pF -27, 500V NPO Ceramic, 1000 pF -103, 500V	D1 D1 D1 C1 C2	03 E2 D2 D3 D1
o A o A o A	C717	24509-0279	Ceramic, 140 pF -55, 500V Ceramic, 2.7 pF -55, 500V Ceramic, 33 pF -57, 500V Tantalom, 2.2 mF -201, 20V Ceramic, 47 pF -56, 500V	C1 C1 C1 C1 C1	D2 C3 C3 C3
o: A o: A o: A	C722 C723 C724	24509-0109 24509-0279 21291-0019	Ceramia, 31 pF -5%, 500V NPO Ceramic, 1.0 pF -5%, 500V Ceramic, 2.7 pF -5%, 500V Ceramic, 1000 pF -10%, 500V Ceramic, 33 pF -5%, 500V NPO	B1 B1 B1 B2 B1	C3 C3 B3 C2 B3
o A	C727 C728 C729	24553-0001 21291-0019 24509-0109	Ceramic, .47pF \(\frac{7}{2}50\), 500V Ceramic, 53 pF \(\frac{7}{2}50\), 500V NPO Ceramic, 1000 \(\frac{7}{2}F = 103\), 500V Ceramic, 1 \(\frac{1}{2}F = 55\), 500V Mica, 47 \(\hbar P = 57\), 300V		B3 B3 B2 B3 A3
			CAPACITOR		
0 A	C732	21296-0006 21296-0006	Mica, 27 pF -51, 500V Ceramic, Fredtaru, 100 pF -107, 250V Ceramic, Feedthru, 100 pF -107, 250V Ceramic, Feedthru, 1000 pf -107, 250V	E1 E1	
			DIODE		
o 7	CR701 CR702	75034-0001 75034-0001	Silicon, Hot Currier Silicon, Hot Currier	D2 B2	F.3
0 A 0 A 0 A 0 A	L702 L703 L704	11798-0002 11485-0034 11451-0048 11870-0002 11870-0002	240 uff Coil, RF	£2 D2 A2 D1	F4 F3 H1 D3
o A o A o A	L707	11870~0002 11870~0002 11870~0002 11870~0002	Coil, RF Coil, RF	C1 C1 B1 A1	C3 C3 B4 B4
			TRANSISTOR		
0 / 0 / 0	Q702 Q703 Q704	75561+0036 75550+0007 75550+0007	Silicon, NPN, 2N3381 Silicon, NPN, 2N4124 Silicon, NPN, 2N3801 Silicon, NPN, 2N3801 Silicon, NPN, 2N3801 Silicon, PNP, 2N5138	D2 C2 C2 C2 A2	F4 F4 F3 G2
0 1 0 0 0 0 1	Q707 Q708 Q709	75622-0001 75622-0001 75622-0001	Silicon, NPN, SRF 215 Silicon, NPN, SRF 215 Silicon, NPN, SRF 215 Silicon, NPN, SRF 215 Silicon, NPN, SRF 215	E1 D1 C1 B1 A1	E2 E2 D2 B3 A3

.1.	ł	Pari	Sumber		1	escri	ption			_
					i i	ESIST	OR			
A A A A	H703 H704	31218 31218 31218	-0174 -0101 -0332	Carbon Carbon Carbon Carbon	Film.	470K 100K	-5% -5%	1 / 4W 1 / 4W 1 / 4W 1 / 4W	D2 D2 C2 C2	E3 F2 G5 G3
A A A A	R706 R707 R708 R709	31218 31218 31218 31218	-0474 -0473 -0231 -0152	Carbon Carbon Carbon Carbon Carbon Carbon	Film, Film, Film,	470K 47K 330	-5%, 5%, 1 5%, 1	1/4W /4W /4W	C2 B2 B2 B2 B2 B2	F2 64 63 63 62
7, 7, 7, 6, 1,	H711 H712 R713 H714	31218 31218 31218 31218	=0331 -0100 -0152	Carbon Carbon Carbon Carbon Carbon	Film, Film, Film,	330 10 1.5K 470E	75% 75% 75%	1/-1W 1/-1W 1/-1W 1/-4W 1/-4W	B2 B2 E1 E1 D1	G2 G3 E2 E3 E1
7. 7. 8. 6. 1.	R717 R718 R718	31218 31218 31218	8-0474 8-0101 8-0152	Carbon Carbon Carbon Carbon Carbon	Film. Film. Film.	170K 100 1.5K	75% 75%	1/4W 1/4W 1/4W 1/4W 1/4W	D1 C1 C1 C1	E2 E3 D1 D2 D3
A A A A A	R722 R721 B724 B725	1 11212 1 11212 1 11212 1 11212	8-0152 8-0174 8-0101 8-0152	Carbon Carbon Carbon Carbon Carbon	Film. Film. Film. Film.	1.5K 470K 100 1.5K	75%, 75%, 75%,	1 / 1W 1 / 1W 1 / 1W 1 / 1W 1 / 1W 1 / 1W	131 131 131 131 142 141 141	C1 C2 B3 B1 B2 A1

NARCO AVIONICS RNAV 860 MODIFICATION INSTRUCTION - 03225-0670

DME 890 MODIFICATION INSTRUCTION FOR MICROPROCESSOR KIT

Purpose: By the installation of this kit, the DME 890 becomes compatible with the RNAV 860.

1.0 PARTS SUPPLIED IN KIT NO. 03225-0500

Item No.	Part Number	Description	Qty
1	74243-0001	Microprocessor and E Prom (38P70)	1
3	42101-0001 04938-0001	40 Pin Carrier Label, DME 890 MOD.	1
4	03225-0670	Modification Instructions (this sheet)	ī

2.0 GENERAL

This Kit contains a microprocessor combined with an E Prom that was specifically designed to permit the Narco Avionics DME 890 to be compatible with the Narco Avionics RNAV 860 Area Navigation System. DME 890's that have this combination installed retain all of their original specifications and may be used as a standard DME without the RNAV 860.

3.0 INSTALLATION

Installing this Kit consists of replacing the original DME 890 microprocessor (U319) with the supplied uP/E Prom combination and a jumper.

3.1 PROCEDURE

- A. Removal of existing uP.
 - 1. Gain access to the DME 890 microprocessor (U319). Refer to the DME 890 maintenance manual. Before removing the old uP, identify and mark Pin #1 PC board hole to facilitate the insertion of the new uP.
 - 2. Cut every pin on the microprocessor as close to the top of the chip as possible. This will leave a pin length long enough to be handled by a long nose plier.
 - 3. While unsoldering each pin, pull the pin from the PC board with the long nose plier as soon as the solder melts.
 - 4. Removing the uP/E Prom combination from its' carrier observe the following caution:

CAUTION

All the standard precautions that apply to the handling of MOS devices should be observed.

3.1 Continued

B. Insertion of uP/E Prom
Identify the location of pin #1 of the uP/E Prom (see
Figure 1) and install the new component by aligning pin
#1 to the previously marked Pin #1 PC board hole.

Using a soldering iron whose tip temperature does not exceed 600°F, solder all 40 pins. Trim the excess pin length from the printed circuit side of the PC board.

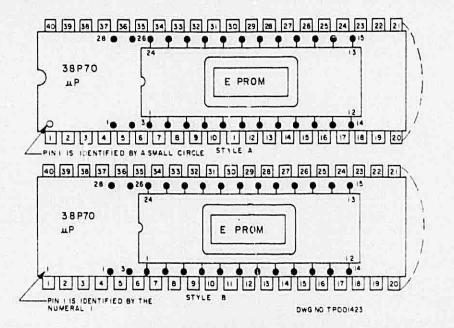
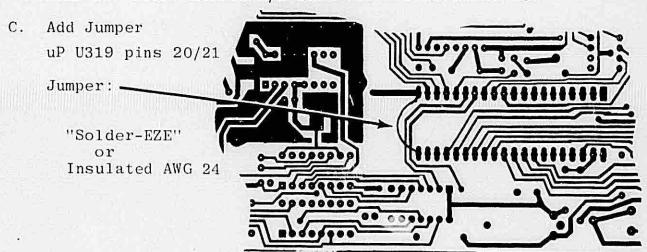


FIGURE 1. MICROPROCESSOR/E PROM PIN 1 IDENTIFICATION



- D. Completion
 - 1. Fasten the RNAV 860 Modification label to the top dust cover of the DME 890. This completes this modification.
 - 2. Bench check the DME 890 according to Section 2 of the DME 890 manual.
 - 3. Bench or ramp test the RNAV 860 system according to the RNAV 860 manual.

NARCO AVIONICS DME 890
MODIFICATION INSTRUCTION: 03314-0670

MODIFICATION INSTRUCTION FOR DME 890 SLIP CODE CHANNELING KIT

KIT NUMBER: 03314-0504

I PURPOSE

To provide detailed instructions to modify a NARCO DME 890 to receive remote channeling information in the form of a SLIP CODE (S/C).

II GENERAL

This modification basically requires the following:

- 1. The layout and connection of eleven (11) jumpers between the S/C Board and the DME's rear connector (P301).
- 2. The layout and connection of a nine (9) wire interconnect cable between the S/C Board and the NAV Unit.
- 3. The check-out of the S/C Board and its installation.
- 4. The removal of the DME and its tray from the aircraft.
- 5. The addition of a Filter Circuit into the DME 890's Main PC Board.
- 6. The re-installation of the Tray, DME, and the connection of the interconnect cable to the NAV Unit.

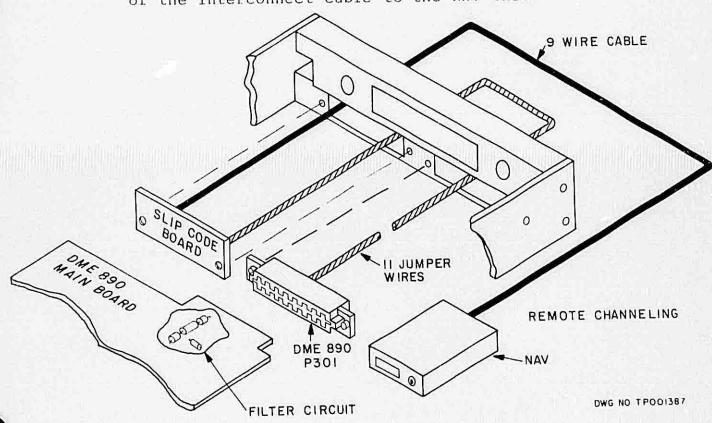


FIGURE 1. SLIP CODE CHANNELING KIT MODIFICATION OVERVIEW

NARCO AVIONICS DME 890
MODIFICATION INSTRUCTION: 03314-0670

III NARCO SUPPLIED ITEMS

The following list of parts may be used to verify the Kits contents:

Item NO.	Narco Part No.	Description	Qty
1	03314-0670	Modification Instruction (this booklet)	. 1
2	01403-1300	Slip Code Channeling PC Board Assy	1 2 3
3	84536-0706	Screw, Mach, Pan Hd, #4-40 x 7/16	. 2
4	81324-0023	Washer, Lock, Split, SS, #4	. 3
4 5	81206-0042	Spacer, .136 ID x .187 OD x .250 long	. 2
6	41407-0002	Pin, Connector	
7	82010-0014	Clamp, Cable	
8	84536-0704	Screw, Mach, Pan Hd, #4-40 x 5/16.	. 1
8 9	81329-0104	Washer, Flat, SS, #4	. 1
10	24551-0002	Capacitor, 470 pF	
11	11485-0016	Choke, 1.8 uH	. 1
12	11454-0003	Ferrite Bead	1000

IV INSTALLER SUPPLIED ITEMS

The following list of items are needed for the modification:

- 1. Standard electrical shop tools.
- 2. A DC voltmeter.
- 3. A DC Power Supply.
- 4. One 4.7K resistor.
- 5. A supply of stranded #22 AWG wire.
- 6. A Molex crimping tool, (See DME Manual Figure 2-10).
- 7. A Molex pin ejector (See DME Manual Figure 2-10).

V PROCEDURE

A. S/C Board to Connector P301 Wiring:

Eleven jumper wires must be soldered to the S/C Board, their opposite ends terminated with a Molex pin connector. These jumpers will be routed to P301 and connected.

- 1. Cut eleven, 6 inch long pieces of stranded #22 AWG wire.
- 2. Refer to Figure 2 and solder one lead to each E1017 thru E1026 and the eleventh to E1029.
- 3. Crimp a Molex pin connector to all these leads except E1025. E1025 will, during installation be connected to P301-10 or -L (GND).
- B. S/C Board to NAV Unit Wiring:

A nine wire cable must be layed out and soldered to the S/C Board, their opposite ends terminated at the NAV Unit.

- Determine the required length of cable between the DME and the NAV Unit, use #22 AWG stranded wire.
- 2. Refer to Figure 2 and solder one lead each to E1002, 4, 6, 8, 10, 12, 14, 16, and 28.

NOTE:

Additional lead connection points (El001, 3, 5, 7, 9, 11, 13, 15, and 27) are available for those installations wherein two NAV Units will be used for channeling. A NAV 1 - NAV 2 switch must be provided (see Figures 8 and 9).

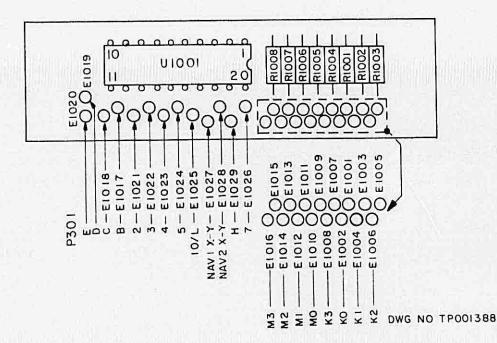


FIGURE 2. SLIP CODE BOARD COMPONENT LAYOUT

C. Pre-Installation Bench Check of the S/C Board.

This check assures that there are no cold solder joints and that the PROM (Ul001) is functioning properly.

- 1. Connect the S/C Board into the test set-up as shown in Figure 3.
- 2. Check each ARINC MHz and KHz code line as follows:
 - a) Refer to Table 1 and ground the appropriate MHz and KHz Slip Code. (These leads are identified by the letter "X")
 - b) Refer to Table 2 and touch each appropriate 2/5 code jumper lead (one at a time) to the test point shown in Figure 3. The maximum permissible voltage is 0.8 Vdc (logic low). The leads are identified by the letter "X". At this time the remaining 2/5 code lines should also be touched to the test point. These leads should indicate an open circuit (voltmeter reads 5 volts).

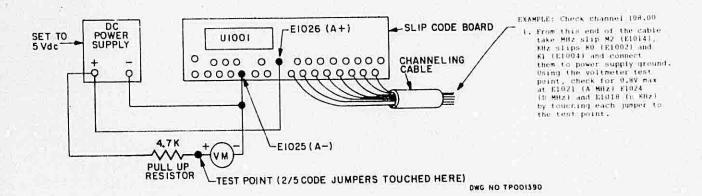


FIGURE 3. SLIP CODE BOARD BENCH TEST SET-UP

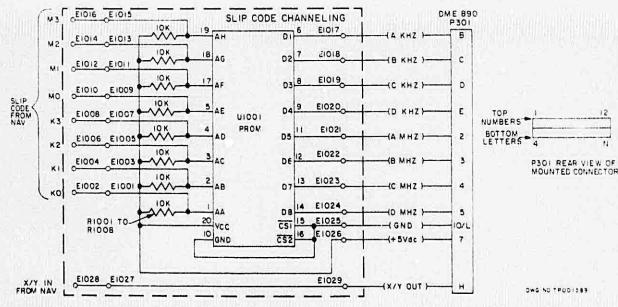


FIGURE 4. SLIP CODE BOARD SCHEMATIC AND INTERCONNECT WIRING

TABEL 1. SLIP CODE DME CHANNEL PROGRAMMING

	SLIP				МН	Z CHANI	NELS				
MHz SLIP	BOARD	108	109	110	111	112	113	114	115	116	117
M _O	E1010			X	x	X		X		x	Х
M	E1012				x	x	x		X -		x
M ₂	E1014	x				х	Х	X		X	
м ₃	E1016		x				X	x	x		x

	SLIP						KI	lz							23433357						
SLIP	CODE BOARD	.00	.05	.10	.15	.20	.25	.30	.35	.40	.45	.50	.55	,60	.65	. 70	.75	.80	.85	.90	.95
κ ₀	E1002	x	х	х	x	x	х	111				x	х							х	X
к,	E1004	x	х	×	x	x	x	У.	х					х	х						
к ₂	E1006	1		х	Х	x	x	х	х	х	x				La V	х	х		, E. U.		
К3	E1008					Х	х	X	х	X	х	×	х					Х	X		
Y CHAN	E1028		Y		Y		Y		Y		Y		Y		Y		Y		Y		Y

NOTES: 1. "X" indicates continuity to system ground 2. "Y" indicates continuity to system ground via NAV Unit

Dwg No. TP001384

TABLE 2. DME 890 AND ARING DME CHANNEL PROGRAMMING

SLIP						MHz (CHANNE	LS				
CODE BOARD	MHz ARINC	DME 890 P301	108	109	110	111	112	113	114	115	116	117
E1021	A	2	X	х		X	х	l, ly-,	ni y	ш,ш,д		
E1022	В	3			X	X		X	X			12.11.11
E1023	С	4					X	X		X	X	-
E1024	D	5	X						X	×		λ.

SLIP	k.=1								KHz	CHAI	NELS	3							-		11.11	112
CODE	KHZ. ARINC	DME 890 P301	.00	.05	.10	.15	.20	. 25	.30	.35	.40	.45	.50	.55	.60	.65	.70	. 75	.80	.85	.90	.95
E1017	A	В			х	х	x	×											х	х	X	Х
E1018	В	С	X	x	X	X			X	X	X	Х	15.11					-			-	-
E1019	С	D					х	х	X	Х			X	X	X	X						
E1020	D	E									X	X	X	X			X	X	X	X		
E1029	Y Chan	н		Y		Y		Y		Y		Y		Y		Y		Y		Y		Y

NOTES:

1. "X" indicates continuity to System Ground
2. "Y" indicates continuity to System Ground via NAV Unit.

Dwg No. TP001383

D. Installation of the S/C Board onto the DME 890 Tray.

It is recommended that the tray be removed from the aircraft for ease of mounting the S/C Board and the routing of its interconnect jumpers and cable.

- If possible do not remove P301 from the tray. Use the Molex Ejector Tool and remove the power leads from P301-9 and -K, also remove the ground leads from P301-10 and -L. If Ident Audio, P301-A was installed, remove this lead also.
- 2. Remove the front and rear tray mounting screws and remove the tray. SAVE THE SCREWS AND OTHER HARDWARE NOTING EACH ITEMS LOCATION FOR EASE OF PROPER RE-INSTALLATION.
- Mount the S/C Board as shown in Figure 5. Note the jumpers and the interconnect cable exit thru the unused connector hole.

THE CABLE CLAMP SUPPLIED MUST BE USED TO RELIEVE WIRE STRESS AT THE S/C BOARD CONNECTION POINTS!

4. With the exception of the ground lead jumper from E1025, connect all the jumpers to P301. Refer to Figure 2 for "E" hole identification and Figure 4 the wiring schematic.

 $\rm E1025$ must be connected to the leads going to $\rm P301-10$ or $\rm -L$ when the tray has been re-installed.

- 5. Replace the tray into the aircraft referring to step 2 (any problems, refer to DME 890 Maintenance Manual's Section 2.5.2).
- 6. Re-connect the power leads P301-9 and -K, the ground leads P301-10 and -L, and the Ident Audio P301A (as applicable).
- 7. Route the NAV Unit channeling cable to the NAV Unit and make the appropriate connections.

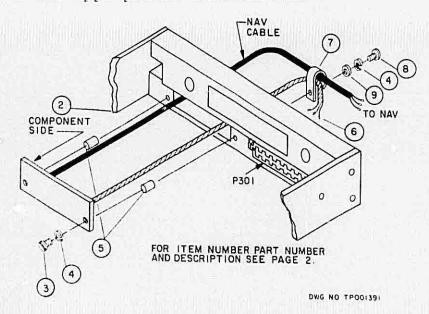
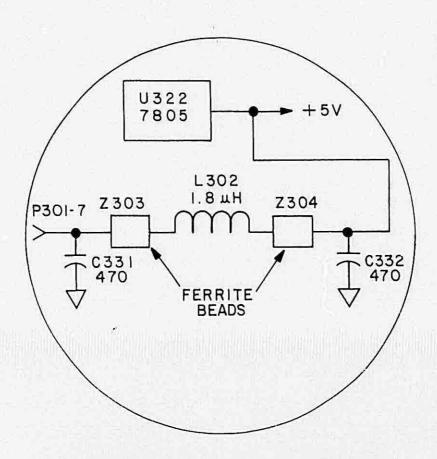


FIGURE 5. INSTALLATION OF THE S/C BOARD TO TRAY

E. MODIFICATION TO DME 890 MAIN BOARD: Figure 6 shows the filter circuit that must be added to the DME 890 Main Board. The Main Board has been produced in two configurations. The installer must determine which of the two configurations, "A" or "B", he has. The means by which the boards are identified is whether there is, or is not, a PC track connected to J301-7. Figure 7 shows board configurations "A" and "B". Both of these configurations show the "component side" of the Main Board in the area of the edge connector J301. All DME 890 components have been deleted from these drawings (except CR301) to avoid confusion. The components shown are those which must be added to the Main Board. The following modifications are for board configurations "A" and "B".



A FILTERED +5V SUPPLY SOURCE FOR THE SLIP CODE PC BOARD IS ADDED TO THE DME 890 MAIN PC BOARD. THE FILTER CONSISTS OF TWO 470 pF CAPACITORS, TWO FERRITE BEADS AND ONE 1.8 LH CHOKE.

FIGURE 6. FILTER CIRCUIT SCHEMATIC

Board Configuration "A" Modification (Figure 7)

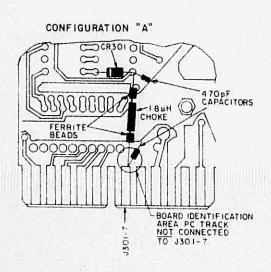
<u>WARNING</u>: This modification requires the soldering of components to the tip of J301-7. Be careful and $\frac{DO\ NOT}{J301-7}$ that mates with the connector.

- 1. Place a ferrite bead on each lead of the 1.8 uH choke.
- 2. Solder the choke between the anode of CR301 and the tip of J301-7.
- 3. Solder one 470 pF capacitor from the anode of CR301 to the Main Board ground plane.
- 4. Solder one 470 pF capacitor from the tip of J301-7 to the Main Board ground plane.

Board Configuration "B" Modification (Figure 7)

Board Configuration "B" will have printed circuit track and mounting holes to accommodate the filter components. Solder the components in the holes provided as shown.

This completes the SLIP CODE channeling Board modification.



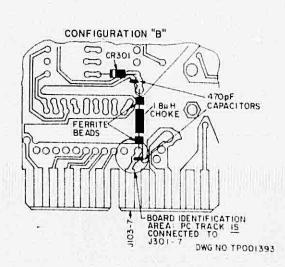


FIGURE 7. DME 890 MAIN PC BOARD (Partial View J301 Area)

F. RAMP/FLIGHT TEST: A ramp or flight test of the system should be performed to verify proper remote channeling of the DME 890.

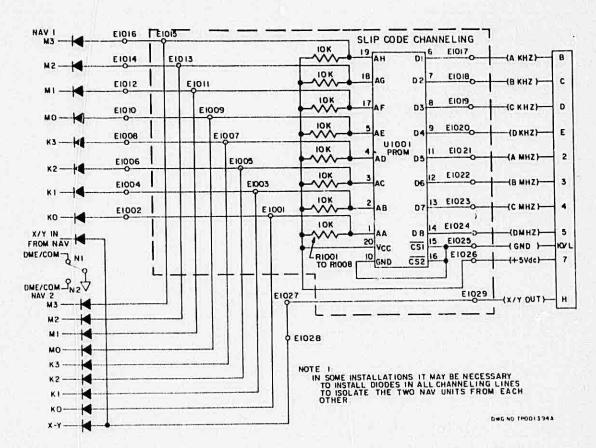


FIGURE 8. NAV 1/NAV 2 SLIP CODE INTERCONNECT DIAGRAM

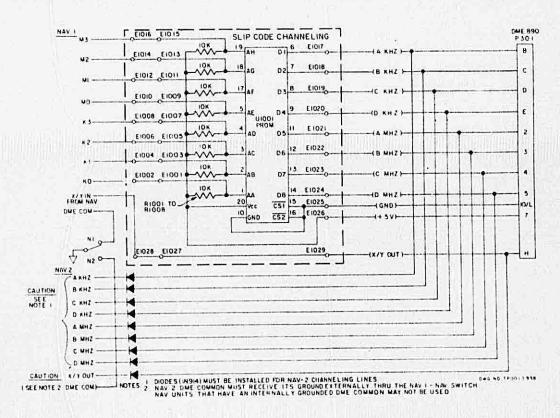


FIGURE 9. NAV 1 SLIP CODE/NAV ARINC CODE INTERCONNECT DIAGRAM

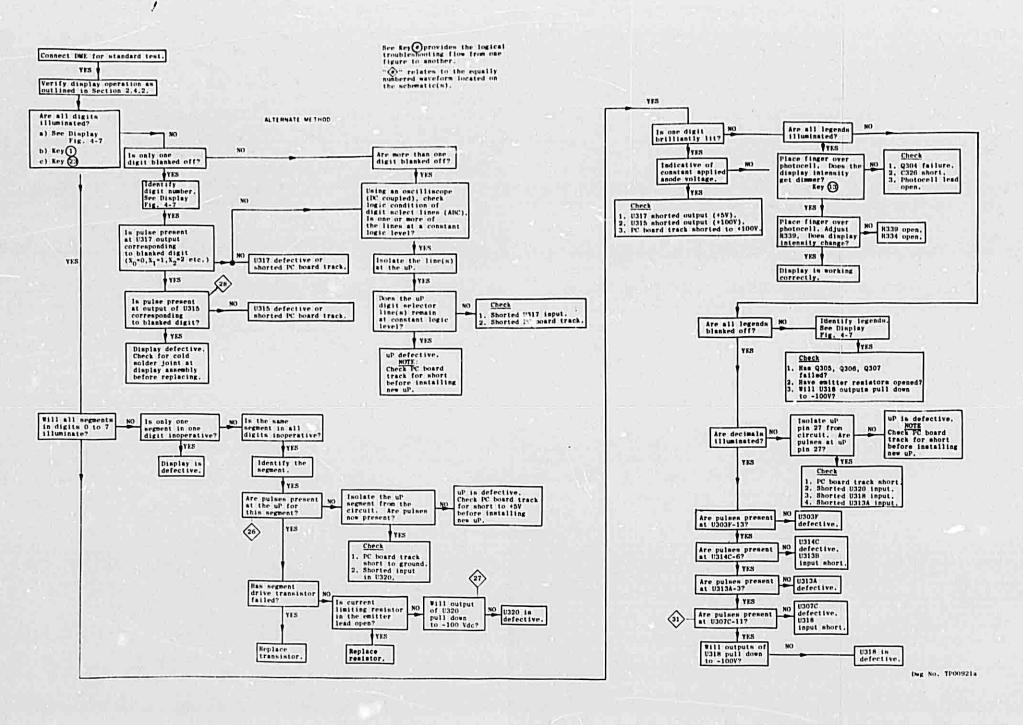
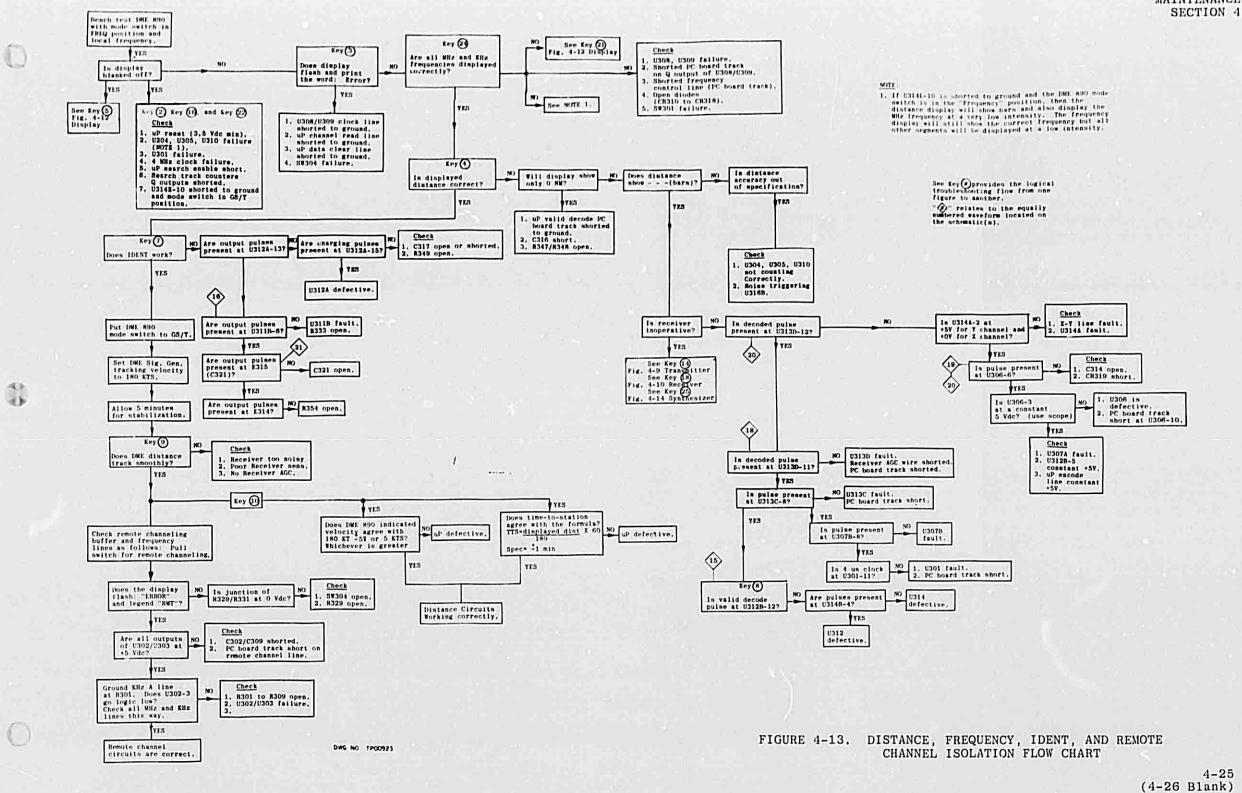
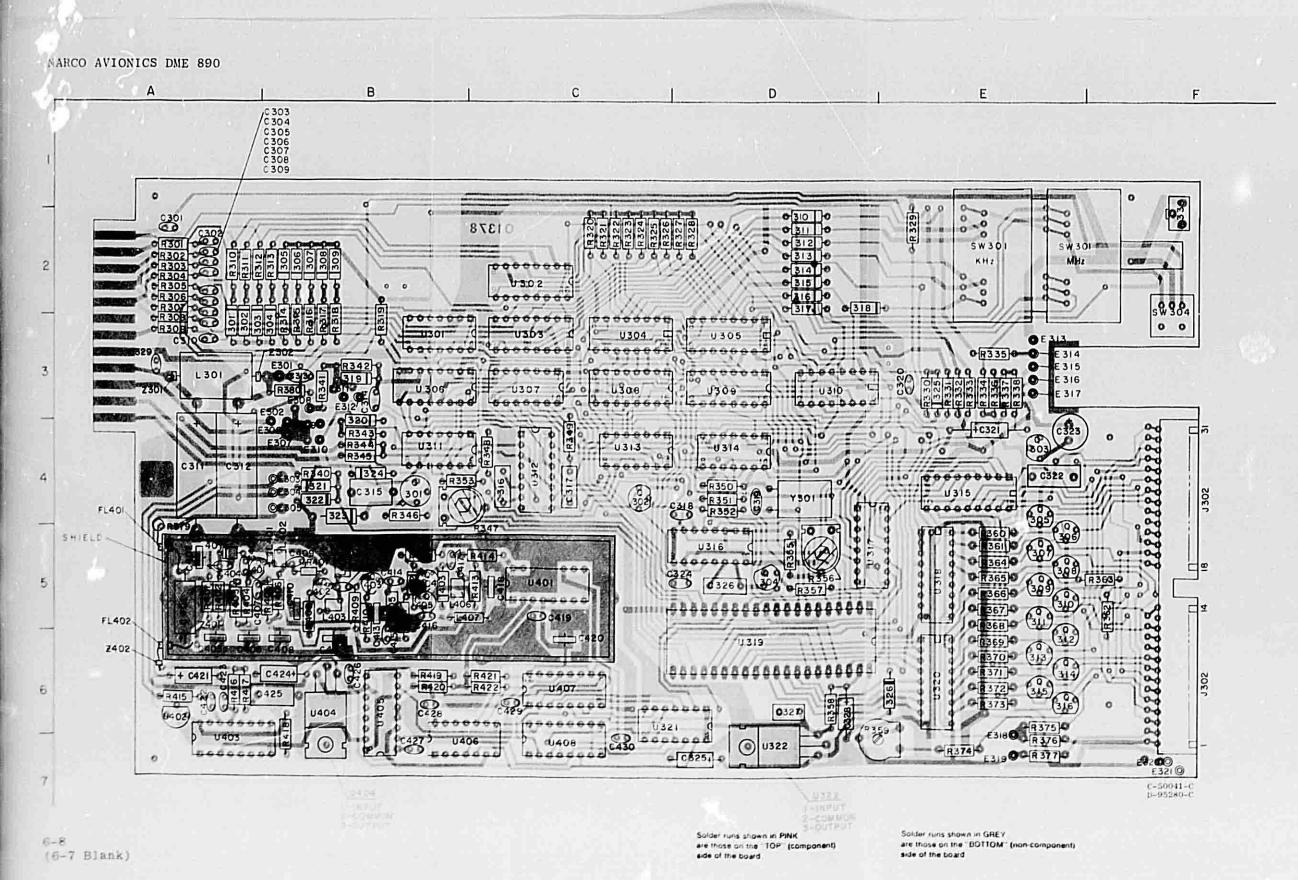
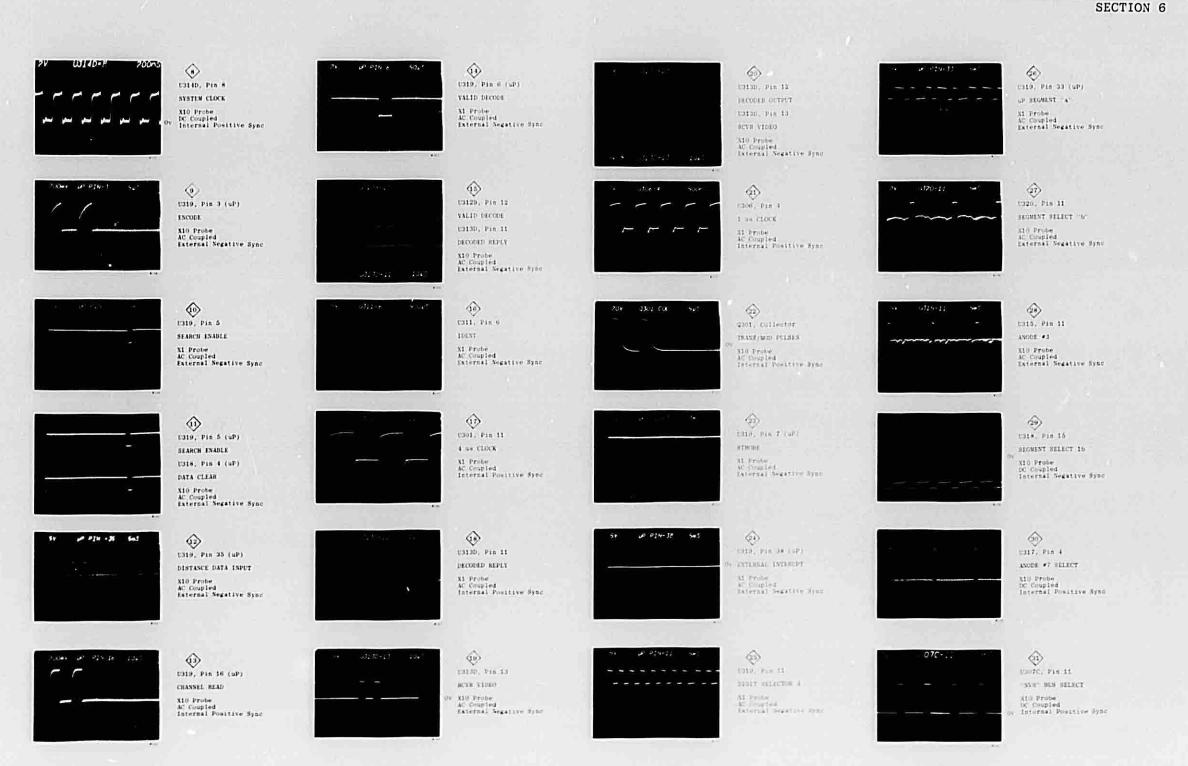


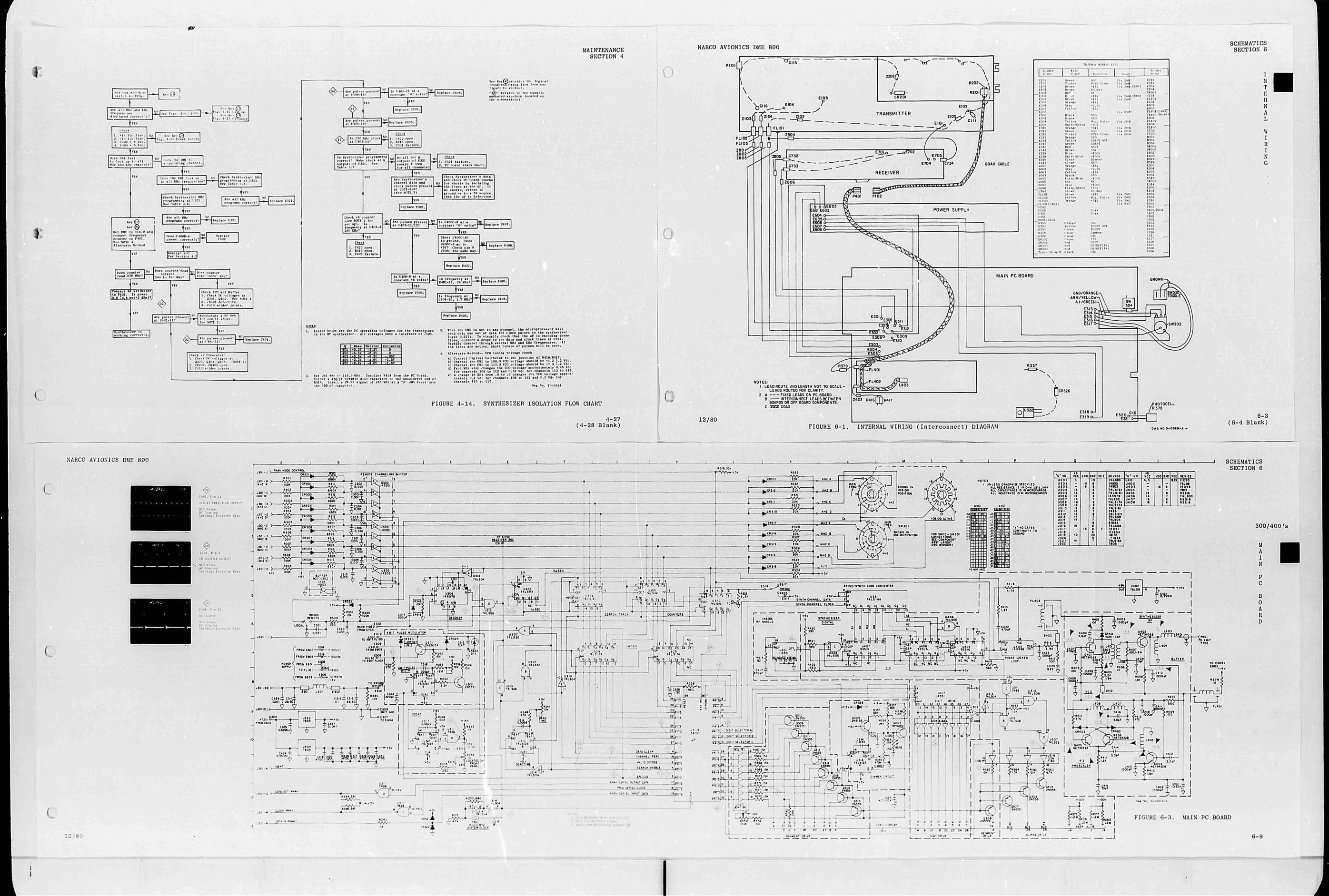
FIGURE 4-12. DISPLAY TROUBLE ISOLATION FLOW CHART ALTERNATE METHOD (sheet 2 of 2) 4-23 (4-24 Blank)



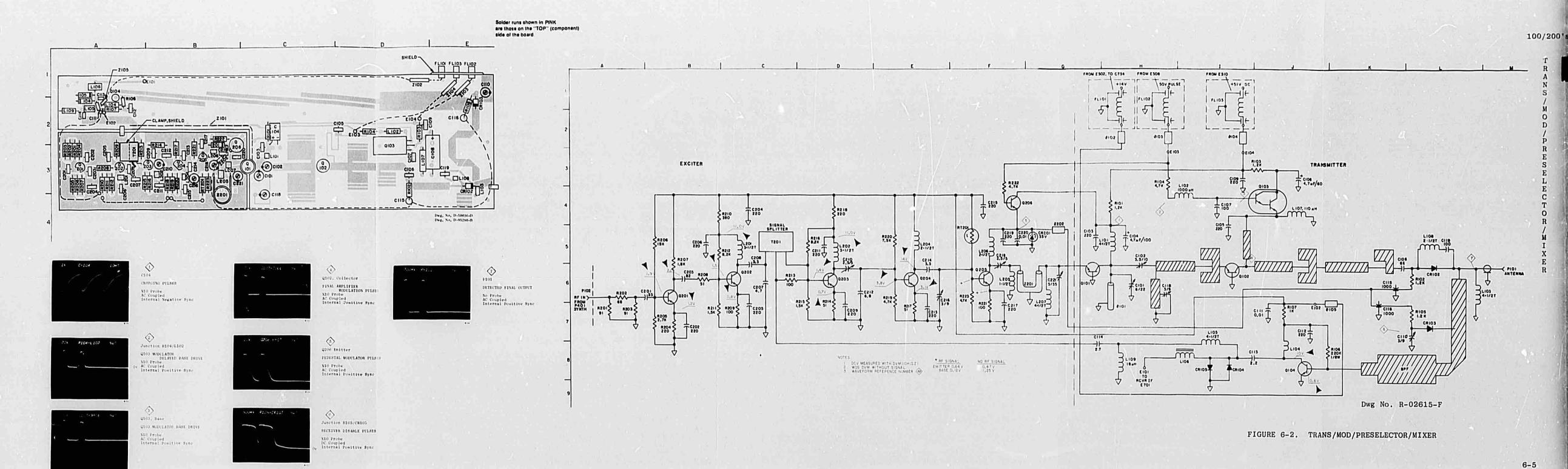




ELECTRICAL PARTS LIST



ELECTRICAL PARTS LIST SECTION 6



NARCO AVIONICS DME 890

12/80

DME 890 ELECTRICAL PARTS LIST LIST NO. 01378-0101M

Ch	on: Original, assis Level Cod Symbol Number	added, changed, deleted. Grid Coc e Component	to diversity of the first	tes c
	Part Numb	er Description		
	1.7-7-10	CAPACITOR		
O A O A	C302 24551-000 C303 24551-000 C304 24551-000 C305 24551-000	5 Ceramic, 1000 pF 10%, 100V 5 Ceramic, 1000 pF 10%, 100V	A2 A2 B1 B1 B1	B6 B1 B2 B2 B2
A A A A A A A A	C306 24551-000 C307 24551-000 C308 24551-000 C309 24551-000 C310 24551-000	5 Ceramic, 1000 pF 105, 100V 5 Ceramic, 1000 pF 103, 100V 5 Ceramic, 1000 pF 103, 100V 5 Ceramic, 1000 pF 105, 100V 5 Ceramic, 1000 pF 105, 100V	B1 B1 B1 B1 A3	B3 B3 B3 B4 B4
O A O A O A	C311 21554-000 C312 21554-000 C313 24550-010 C314 24052-020 C315 23113-010	6 Electrolytic, 25 mF +107 -1509, 50V 6 Electrolytic, 25 mF +101 -1501, 50V 4 Ceramic Mono, 0.1 mF -207, 100V 1 Mica, 200 pF -57, 300V 3 Wetzl Poly 0.47 mF -107, 100V	A4 B3 B3 B4	B8 B8 C6 D7
O A O A O A	C316 23107-001 C317 23107-000 C318 24052-022 C319 24052-8EI	0 Poly Film, 0056 mF +5%, 100V 5 Poly Film, 0022 mF -5%, 100V 1 Mica, 220 pF -5%, 300V Mica, SFL -5%, 300V	C4 C4 D4 D4	F9 C9 C7 E13 B6
0 A 0 A 0 A 0 A	C321 21568-106 C322 23113-010 C323 21567-002 C324 24052-022 C325 21568-107	5 Ceramic, 001 mf -103, 100V 2 Tantalum, 10 mf -203, 20V 1 Metal Poly, 0.22 mf -103, 100V 4 Electrolytic, 1.7 mf +755 -183, 100V 4 Tantalum, 0.33 mf -205, 200V 9 Poly Film, 33 mf -205, 20V 0 Tantalum, 1 mf -205, 20V 0 Tantalum, 1 mf -205, 20V 0 Tantalum, 1 mf -205, 20V	E4 E4 E4 D5	D10 L10 M12 C8 A10
O A O A	C326 23107-001 C327 24550-047 C328 21568-108 C329 24551-00	9 Poly Film, .33 mF 25%, 03V 3 Ceramic, Mono, .047 mF -10%, 100V 0 Yantalum, 1 mF -20%, 20V 5 Ceramic, .001 mF -10%, 100V	D5 D6 D6 A3	110 B9 H8 A9
		CAPACITOR		
o A	C401 21568-109 C402 24562-003	2 Tantalum, 10 mF *20%, 20V 2 Ceramic, Trapezoid, 1000 pF *80% -20%, 65V		812
0 A			A5	
n A	C404 24552-156 C405 24552-123	1000 pF.+807207, 63V 9 Ceramic. 5.6 pF 1.5 pF. NFO. 50V 9 Ceramic. 2.2 pF5 pF. NFO. 50V	A5 A5	Q6 R7
1.	F408 945892001	2 Ceramic Traperoid, 1000 pF 1801 -20%, 63V 2 Ceramic, 470 pF -20%, 50V 2 Ceramic, Trapezoid,		Q8 Q7
O.A	C409 24552-115	0 Ceramic Trapezoid, 15 pF -10% 50V	BG B5	Q8 B7
01A	C410 24562+90.	2 Ceratic, Trapezoid, 1000 pF +80% -20%, 639		8.8
e/A		2 Ceramic, Trapezoid, 1000 pE +809 -200 635	86	89
		9 Keramin, Trapezorid, 2,2 pF - 5 pF, NPO, NO.	B5	811
A	C410 24562-000		B6 B5	B11 B10
in A	C415 24552-133	1000 pt -80% -20% M3V 1000 pt -80% -20% M3V 19 Coramic, 3/3 pf -5 pf 50V 550 10 Coramic, 3/3 pf -5 pf 50V 500	1945	R12
O.A. O.A.	C416 24052-156 C417 24551-000 C418 24562-003	9 Ceramic, 5.6 pF 2.5 pF, 50V, NFO 2 Ceramic, 170 pF -20%, 50V 2 Ceramic, Trapezoid	B5 B5	38
0.A	C419 24550+041	1000 nF +800 -200 CNV 2 Ceramic0047 nF -205 100V 2 Ceramic Trapecold	C5 C5	R11
		1000 pf 4805 -207 00V	ce	B11
O A	0422 24001-000 0423 24001-000 0424 21508-10	4 Tantalus, 0.32 eF \$205, 207 2 Ceramic, 470 pF \$205, 50V 5 Ceramic, 1000 pF \$105, 1000, 4 Ceramic, Tantalus, 0.33 eF \$20, 20V 1 Mets! Poly, 0.22 eF \$105, 1006	A6 A6 A6 B6 B6	95 95 97 A10 97

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					CA	PACITOR				
0 0 0	A	C427 C428 C429	24550-0472 24550-0472 24550-0472 24550-0472 24550-0472	Ceramic, Ceramic,	Mono. Mono.	.0047 mF	-20%	100V 100V 100V 100V 100V	B6 B7 B6 C6 C7	B11 B11 B11 C11 C11
					<u>D10</u>	ODE				
0 ,	ACAC	R302 R303 R304	75028-0001 75028-0001 75028-0001 75028-0001 75028-0001	Silicon, Silicon, Silicon,	Switch Switch Switch	hing, 25V hing, 25V hing, 25V			A3 A3 A3 A3 B2	A1 A2 A2 A2 A1
0 /	A C	E307 E308 E309	75028-0001 75028-0001 75028-0001 75028-0001 75028-0001	Silicon, Silicon, Silicon,	Switch Switch Switch	hing, 25V hing, 25V hing, 25V			82 83 82 82 82	A3 A3 A3 A2 K2
000	A C	R312 R313 R314		Silicon, Silicon, Silicon,	Switch	hing, 25V hing, 25V hing, 25V			D2 D2 D2 D2 D2	K2 K1 K1 K1 K3
0 /	1 0	R317	75028-0001 75028-0001 75028-0001 75028-0001 75046-0001	Silicon.	Switc.	hing, 25V	1 mA		D2 D2 D2 B3 B4	K3 K3 K4 C6 C7
00000	1 0	R321 R322 R323 R324 R325	7502F-0001 75028-0001 75047-0007 75028-0001 75028-0001 75028-0001	Silicon, Silicon, Zener, 5 Silicon, Silicon,	Switch Switch IV. 15 Switch Switch	hing, 25V hing, 25V hing, 25V hing, 25V			B4 B4 B4 B4 E3 E6	C13 C13 D7 D7 B5 L9
					D1	ODE				
0	A I	31402	75043+0001 75028-0001 75028-0001	Silicon.	Swite	hing, 25V hing, 25V			A5 B5 B5	R6 R6 Q10
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A A A A	Q302 Q303 Q304 Q305	75675-0001 5 75676-0002 5 75596-0001 5 75675-0001 5	Silicon, PNP, 2 Silicon, NPN, 2 Silicon, PNP, M Silicon, PNP, 2 Silicon, NPN, 2	N2905A N5551, 140V PSA92, 200V N5138 N5551, 140V	B4 C4 E4 D7 E1	D7 D8 M10 L9 Q12
AAAA AAAAA	Q309 Q310 Q311 Q312 Q313 Q314 Q315	75675-0001 5 75675-0001 5 75675-0001 5 75675-0001 7 75675-0001 7 75675-0001 7 75675-0001 7	Silicon, NPN, 2	N5551, 140V N5551, 140V	E5	P12 P12 N13 K9 K9 K10 K10 L11 L12 L12
AAAAAAA	Q102 Q103 Q104	75677-0001 5 75677-0001 5 75677-0001 5	dicrowave, NPN, dicrowave, NPN, dicrowave, NPN, dicrowave, NPN, dicrowave, NPN,	NEC73432B NEC73432B NEC73432B NEC73432B NEC73432B	85 85	Q7 R6 R11 R10
				1 STOR		
AAAAA	R301 R302 R303 R301 R305	31218-0104 (31218-0104 (31218-0104 (31218-0104 (31218-0104 (arbon Film, 10 arbon Film, 10 arbon Film, 10 arbon Film, 10 arbon Film, 10	OK 559, 1/4 OK 559, 1/4 OK 559, 1/4 OK 559, 1/4 OK 559, 1/4 OK 571, 1/4	A2 A2 A2 A2 A2 A2 A2	A1 A2 A2 A2 A2
AAAAA	E306 E307 E308 E309 E310	31218-0104 (31218-0104 (31218-0104 (31218-0104 (31218-0684 (arbon Film, 10 arbon Film, 10 arbon Film, 10 arbon Film, 10 arbon Film, 68	OK 57, 1/40 OK 57, 1/40 OK 57, 1/40 OK 59, 1/40 OK 57, 1/40	A2 A2 A3 A3 A2	A3 A4 A4 A4 B1
A A A A	R311 R312 R313 R314 R315	31218-0684 (31218-0684 (31218-0684 (31218-0684 (31218-0684 (arbon Film, 68 arbon Film, 68 arbon Film, 68 arbon Film, 68 arbon Film, 68	OK :5%, 1/40 OK :5%, 1/40 OK :5%, 1/40 OK :5%, 1/40 OK :5%, 1/40	A2 A2 A2 B3 B3	B1 B2 B2 B4 B3
A A A A	H316 H317 H318	31218-0684 (31218-0684 (31218-0684 (arbon Film, 68 arbon Film, 68 arbon Film, 68	OK +5% . 1/40 OK +5% . 1/40 OK +5% . 1/40	B3 B3 B3	B3 B3 B2 J1 K2
AAAAA	8321 8322 8323 8321 8325	31218-0203 (31218-0203 (31218-0203 (31218-0203 (31218-0203 (arton Film, 20 arton Film, 20 arton Film, 20 arton Film, 20 arton Film, 20 arton Film, 20	K 151, 1/4W K 151, 1/4W E 155, 1/4W K 157, 1/4W K 157, 1/4W	C2 C2 C2 C2 C2 C2	K2 K1 K1 K1
AAAAA	-R326	31218-0203 (arbon Film, 20 arbon Film, 20 arbon Film, 20 arbon Film, 22 arbon Film, 10	K -51, 1/4W	C2	K3 K3 K3 B6 B6
AAA	8331 8332 8333	31218-0103 0 31218-0222 0 31218-0102 0	arbon Film, 10 arbon Film, 2 arbon Film, 18 arbon Film, 10 arbon Film, 13	6 - 9% 1 / 48 26 - 5% 1 / 48 - 5% 1 / 48		
			arton Film. 24 arton Film. 30 arton Film. 5. artable. 4708 arbon Film. 18		E3 E3 E3 F2 64	

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-			Part Number	Description		
	•			RESISTOR		F
000	A	R3 14	31218-0391 Carbon 31218-0391 Carbon	Film, 390 -5%, 1/4W Film, 390 -5%, 1/4W	84 84 84	C7 C5 D7 B1 B1
0	AAAA	R346 R347 R348 R349 R350	31218-0103 Carbon 32075-0004 Variabl 31218-0273 Carbon 31218-0104 Carbon 31218-0681 Carbon	Film, 10K -57, 1/4W e Cermet, 10K Film, 27K -57, 1/4W Film, 100K -57, 1/4W Film, 680 -57, 1/4W	84 C5 C4 C4 D4	D7 F9 E9 D9
	AAA	3319393	Dieta-0125 Carbon	Film, 47K -52, 1/4W Film, 2:2E -5%, 1/4V Film 10K -53, 1/4W e w/Switch_SW303 (OI Film, 12K -53, 1/4W	Da	D1 D8 P9 D1 D7
O	A	R359	32054-0012 Variabl 31218-0172 Carbon	e Cermet, 10K Film, 68K -57, 1/4W Film, 1 Meg -5%, 1/- e, 100K Film, 4.7K -5%, 1/-4V Film, 12.0K -5%, 1/-4V	D6 D6 E5	D7 L9 H8 J1 Q1
0	AAAAA	R362 R363 R364 R365	31218-0203 Carbon 31218-0125 Carbon 31218-0752 Carbon 31218-0153 Carbon	Film, 10K -5%, 1/W Film, 1.2M -5%, 1/W Film, 7.5K -5%, 1/W Film, 7.5K - 5%, 1/W	F5 F5 E5	P1 K1 R1 P1 N1
		11310	Sizio-Oisa Carbon	Film, 15K +5%, 1/4W Film, 15K +5%, 1/4W Film, 15K +5%, 1/4W Film, 15K +5%, 1/4W Film, 15K +5%, 1/4W	E5 E5 E5 E6 E6	J1 J1 J1 J1
0 0	AAAAA	R371 R372 R373 R374 R375	31218-0153 Carbon 31218-0153 Carbon 31218-0153 Carbon 31218-0103 Carbon 31218-0105 Carbon 31218-0125 Carbon	Film, 15K -5%, 1/4W Film, 15K -5%, 1/4W Film, 15K -5%, 1/4W Film, 10K -5%, 1/4W Film, 1,2W -5%, 1/4W	E6 E6 E7 E7	J1 J1 J1 J1 Q1
0 0 0	AAAAA	R377	31218-0125 Carbon 31218-0125 Carbon	Film, 1.2M ±5%, 1/48 Film, 1.2M ±5%, 1/48 Film, 10 ±5%, 1/48 Film, 10K ±5%, 1/48	E7	Q1: Q1: T8
ö	AAAAA	R401 R402 R403 R404 R405	31218-0103 (Arbon 31218-0103 (Arbon 31218-0103 (Arbon 31216-0222 (Arbon 31218-0751 (Arbon 31218-0101 (Arbon	Film, 108 -5% 1/4W Film, 560 5% 1/4W Film, 108 -5% 1/4W Film, 2,2K -5% 1/8W Film, 750 5% 1/4W Film, 100 -5% 1/4W	B3 A5 A5 A5 A5 B5	C8 Q6 R8 Q7 Q8
o.	AAAAA	R406 R407 R408 R409 R410	31218-0102 Carbon 31218-0101 Carbon 31218-0182 Carbon 31218-0101 Carbon 31218-0182 Carbon	Film, 1K -5%, 1/4W Film, 100 -5%, 1/4W Film, 1.8%, -5%, 1/4W Film, 100 -5%, 1/4W Film, 1.8K -5%, 1/4W	B5 B5 B5 B5 B5	R8 R7 R8 S9 R1
0	AAAAA		area or or carbon	Film, 1.2K -5%, 1/4W Film, 470 -5%, 1/4W Film, 470 -5%, 1/4W Film, 82 -5%, 1/4W Film, 1.8K -5%, 1/4W	Att	R1: R9 Q9 J7 P5
9	AAAAAA	R416 R417 R418 R419 R420 R421 R422	31218-0392 Carbon 31218-0331 Carbon 31218-03472 Carbon 31218-0561 Carbon 31218-0391 Carbon 31218-0391 Carbon 31218-0391 Carbon	Film, 3.9K, 253, 1/4W Film, 330 - 52, 1/4W Film, 4.7K, 55, 1/4W Film, 560 - 51, 1/4W Film, 390 - 52, 1/4W Film, 390 - 53, 1/4W	A6 A6 B7 B6 B6 C6 C6	Q7 Q7 P5 N7 K6 K7 K1
				SWITCH		
Ε,	A.	5¥302	61658-0001 Hotary.(61497-0007 Toggle. (0%/OFF- 61646-0001 Slide Hr	Frequency) (MHz-GS/T) Part of R354, IDENT Angle (Remote Freq		M3 K5 D11 A6

	Symbo	1 Number	Component A	l l	
u	•	Part Number	Description	_	•
			<u>1C</u>		
	U301 U302	74048-0002	4 Bit Binary Cntr 74LS93 (LST ² L) Hex Tri-State Buffer 14503 (CMOS)	B3 C2	E5
0.1		11213-0001			C1 C1
	U302C				C2
0 /	U302D				C2 C4
0 A	U302F	74213-0001	Hex Tri-State Buffer 14503 (CMOS)	СЗ	C4
o A	U303A				C4
	U303B				C3 C3
3 /	U303D U303E				C3 B4
	U303F				N9
	U304	74043-0002	Synchronous 4 Lit Binary Cntr 74LS161 (LST"L)	СЗ	F5
0.1	U305	74043-0002	Synchronous 4 Bit Binary Cntr 74LS161 (LST*L)	D3	G5
o A	U306	74217-0001	1/64 Bit Variable Length S/R 14557B (CMOS)	В3	D5
6 U	U307		Quad 2 Input OR Gate 74LS32 (LST ² L)	C3	
5 1	U307A U307B				E7 E8
	U307C				Q10
0 /	U308 U309	74176-0001 74176-0001	Hex D-Flip-Flop 74LS174 (LST ² L) Hex D-Flip-Flop 74LS174 (LST ² L)	D3	G7 H7
	U310	74043-0002	Synchronous 4 Bit Binary Cntr 74LS161 (LST L)	рз	J5
0 /	U311	74231-0001	Quad 2 Input NAND Gate H: Volt, 7426TTL	84	
0 A	U311A U311B				D10
0 0	1311C				C12
o A	U311D	74062-0002	Dual S.S. Multi 74LS123 (LST2L)	C4	P8
	U312A U312B				D10 E10
5 A	U313	74024-0002	Quad 2 Input AND Gate 74LS08 (LST2L)	C4	
	U313A U313B				P9 P9
	U313C				ES E5
o A	U314	74051-0003	Hex Inverter 74LS04 (LST ² L)	D4	
	U314A U314B				D4 E11
0 A	U314C				N8 E12
	U314E U314F				F8 D13
		74216-0001	Octal Hivoltage Digit Driver UDN6184A	E4	11.0
o UA	U315A U315B	V2012		TATE OF	N9
0.4	U316A	74062-0002	Dual S.S. Mult: 74LS123 (LST ² L)	D5	C8
	C316B				111
o . A	U317		8 Bit Multiples/Dimultiples 14051 (CMOS)	D5	N8
o A	U318 U319	74214-0001	Octal HiVoltage Seg. Driver UDN7180A Microprocessor, 3872	E5 D6	Q11 H10
a A	U320 U321	74215-0001 74170-0001	Octal Hivoltage Digit Driver UDN7180A IN/P. OUR Shift Reg., 74LS164 (LST°L) 5V Regulator, -21 1 Amp, 7805	E6 C6	J12 L5
	U322	74039-0102	5V Regulator, -21 1 Amp, 7805	D7	A9

c	Chassis	original, ac Level Code 1 Number	ided, <u>c</u> hanged, <u>d</u> eleted, <u>Grid Coor</u> Sche Component A	muti	
	•	Part Number	Description	•	•
	A U401	74068-0003	UHF High Speed Prescaler, 11C90	C5	K7
	A U402	74109-0002	8V Reg., 10-mA, 78L08	A6	R5
	A U403	74119-0001	Phase Locked Loop, 4046B (CMOS)	AG	P7
	A U404 A U405	74039-0002 74218-0001	5V Regulator, -4% 1 Amp, 7805 Synchronous, 4 Bit Binary Cntr	B6	A10
			93S16 (ST ² L)	B6	N7
	A U406	74019-0002	Quad, 2 Input NAND Gate 74LS00 (LST2L)	В7	
	A U406A A U406B				va
	A U406C				N6 L7
	A U407	74218-0001	Synchronous, 4 Bit Binary Cntr		
	A CIOI	7-1410-0001	93S16 (ST ² L)	C6	L7
	A U408	74218-0001	Synchronous 4 Bit Binary Cntr	-	
		11210-0001	93S16 (ST ² L)	C7	М7
			CRYSTAL		
	A Y301	72064-0001	Quartz, 4,000 MHz	D4	D1 3
			BEADS		
	A Z301	11454-0003	Ferrite Bead	A3	A8
	A 2302	11454-0003		B3	B8
	A 2401		Ferrite Bead	A5	SB
	A 2402	11454-0003	Ferrite Bead	AG	R6

6-10

10.100

2.5.4 Antenna

The Blade antenna, type UDA-3, is used for both receiving and transmitting by the DME. This antenna should be mounted on the bottom surface of the aircraft and located so that it is in the vertical position when the aircraft is in a level flight attitude. The mounting surface should be metal, electrically grounded, and extend at least 6" in all directions from the antenna connector. (See Figure 2-11). A three (3) foot minimum separation from other antennas, particularly transponders should be maintained.

Avoid mounting the antenna in the vicinity of aircraft protrusions as this is likely to create some radiation "shadowing" with a resultant loss in signal strength from both transmitted and reply signals.

If this antenna is to be used on non-metallic aircraft skin, a ground plane at least 6" in diameter must be provided. This could be as simple as aluminum foil cemented inside a wood or fiberglass skin, or a doubler plate on a fabric-covered aircraft. Such a ground plane should be either well bonded to the airframe, or well insulated from it, to prevent erratic operation.

A doubler plate will be needed for an airworthy installation on most aircraft. Check the airworthiness regulations of the country of aircraft registry for acceptable mounting methods. Figure 2-11 is removable for a drilling template.

DO NOT PAINT. other finish.

This antenna may not be coated with any paint or 6"RADIUS, MIN (15 cm)

USC DONAL SIZE 18 (190 MOLE) (17/32 CLEARANCE MOLE RECOUNTD FOR MOUNTING FOR MOUNTING (22.2mm)

UDA-3 (102 mm) (103 mm)

UDA-3 (103 mm) (104 mm) (105 mm)

(104 mm) (105 mm) (105 mm) (105 mm) (105 mm)

(105 mm) (105 mm

12/80

0

FIGURE 2-11. UDA-3 ANTENNA

2-15

4-17

FULL SIZE V TEMPLATE

PANEL CUT-OUT TEMPLATE

INSTALLATION SECTION 2

PANEL CUT-OUT TEMPLATE

INSTALLATION SECTION 2

INSTALLATION DRAWING

(2-8 Blank)

NARCO AVIONICS DME 890

4.8 WAVEFORMS

Waveforms and test locations are identified on the schematics in Section 6 by means of a reference number in a diamond-shape enclosure. These waveforms are also referenced in the trouble-shooting flow charts Figures 4-8 thru 4-14.

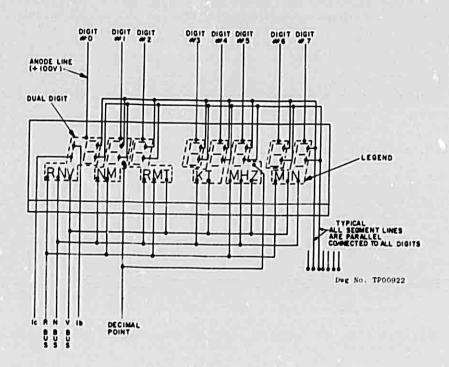


FIGURE 4-7. GAS DISCHARGE DISPLAY INTERNAL WIRING

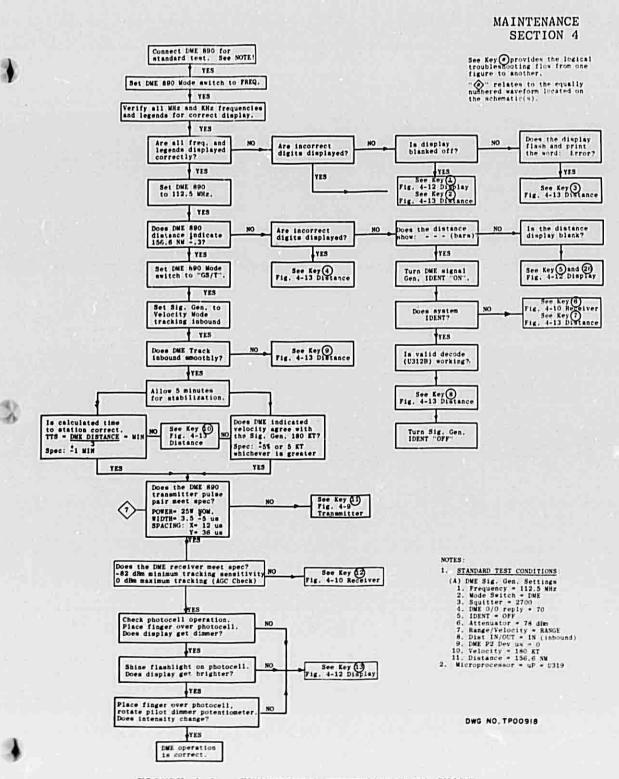
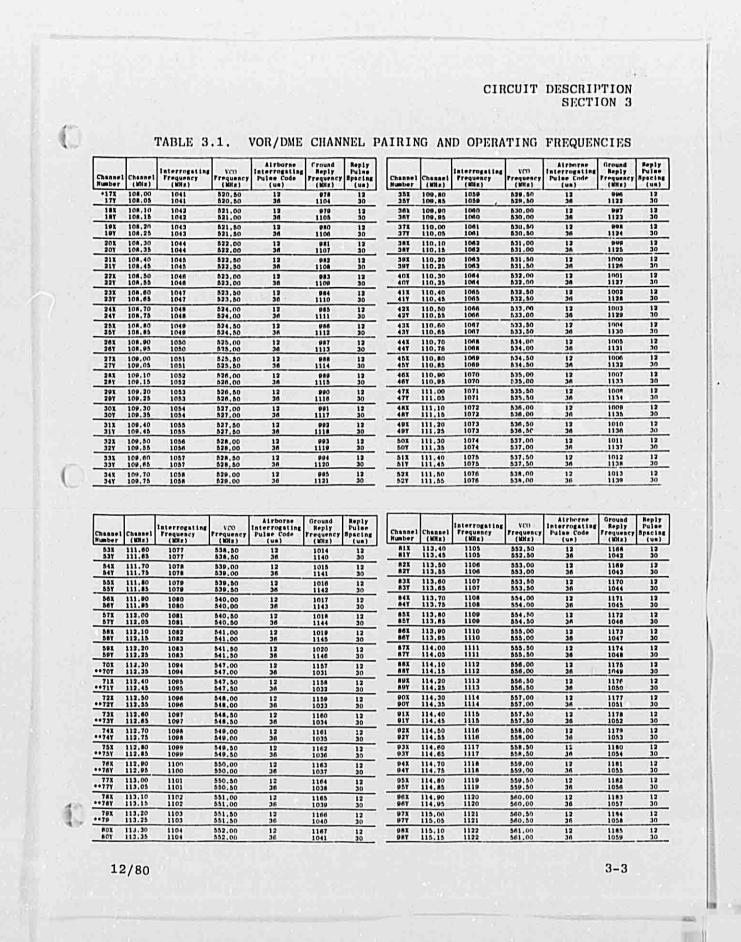
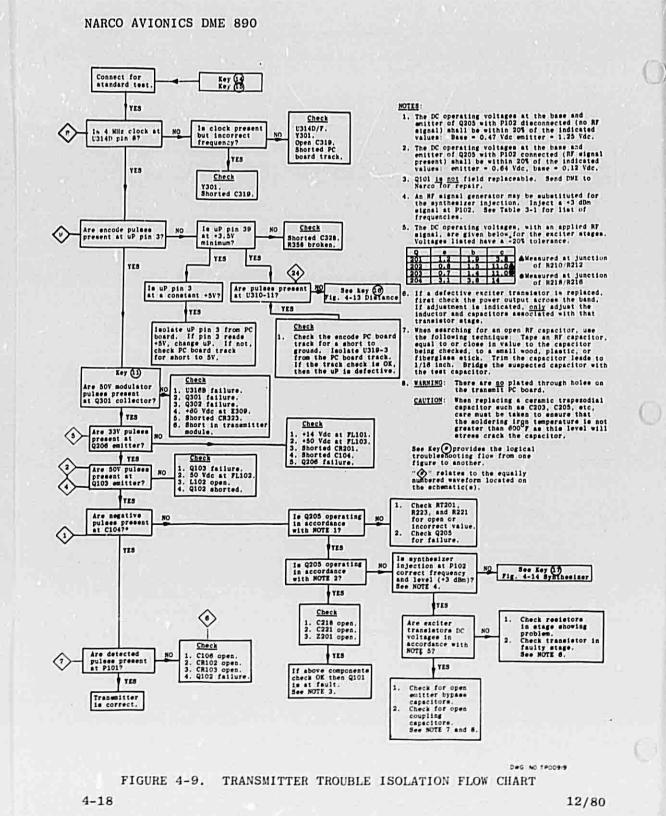
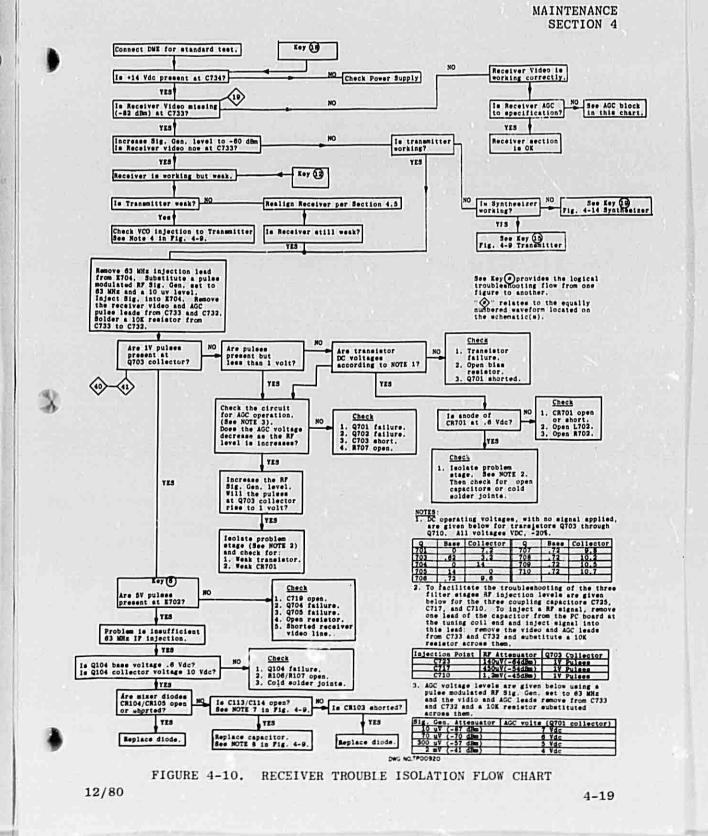


FIGURE 4-8. FUNCTIONAL CHECKOUT FLOW CHART







Replace Capacitor

FIGURE 4-11. POWER SUPPLY TROUBLE ISOLATION FLOW CHART

Power supply is check for open rectifier diode.

"A" relates to the equally numbered waveform located on the schematic(s). THE PROPERTY OF THE PROPERTY O

FIGURE 4-12. DISPLAY TROUBLE ISOLATION FLOW CHART (sheet 1 of 2)

4-21 (4-22 Plank)

MAINTENANCE SECTION 4

